



## STP120NF04

N-channel 40V - 0.0047 $\Omega$  - 120A TO-220  
STripFET™ II MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP120NF04	40V	<0.0050 $\Omega$	120A	300W

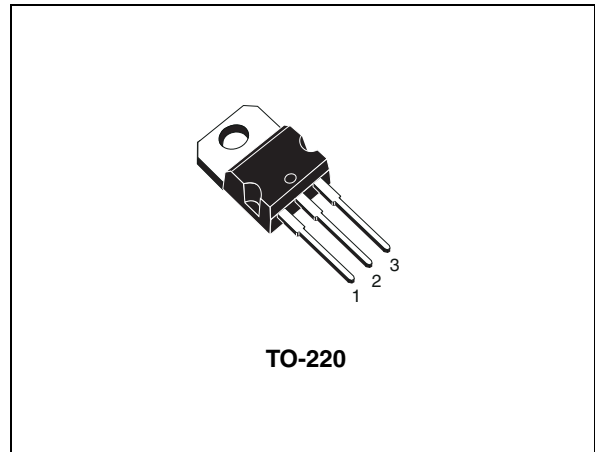
- Standard threshold drive
- 100% avalanche tested

### Description

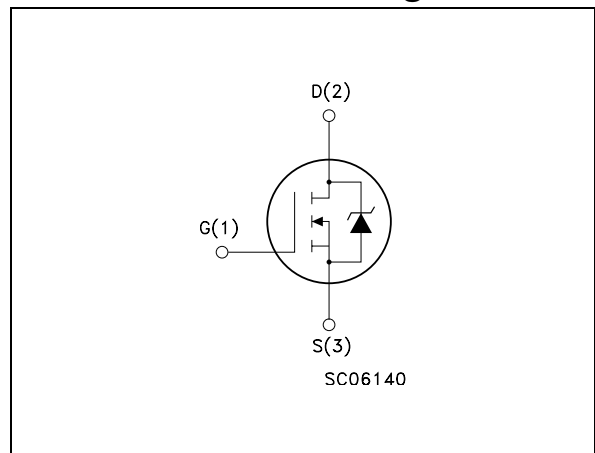
This MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STP120NF04	P120NF04	TO-220	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	120	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	480	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	300	W
	Derating factor	2	W/°C
$dv/dt^{(3)}$	Peak diode recovery voltage slope	6	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.2	J
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	°C

1. Current Limited by Package
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 20\text{A}$ ,  $di/dt \leq 300\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$ .
4. Starting  $T_J = 25^\circ\text{C}$ ,  $I_d = 60\text{A}$ ,  $V_{DD} = 30\text{V}$

**Table 2. Thermal data**

$R_{thj-case}$	Thermal resistance junction-case Max	0.5	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb Max	see <a href="#">Figure 14. on page 8</a>	°C/W
$R_{thj-a}$	Thermal resistance junction-ambient (free air) Max	62.5	°C/W
$T_I$	Maximum lead temperature for soldering purpose	300	°C

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	40			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating},$ $T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.8		4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 50 A$		0.0047	0.0050	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 50A$		150		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		5100 1300 160		pF pF pF
$t_{d(on)}$ $t_r$	Turn-on delay time rise time	$V_{DD} = 20 V, I_D = 60 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 18)		35 220		ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time fall time	$V_{DD} = 20 V, I_D = 60 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ (see Figure 18)		80 50		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 32V, I_D = 120A$ $V_{GS} = 10V$ (see Figure 19)		110 35 35	150	nC nC nC

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 5. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				120	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				480	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=120A, V_{GS}=0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD}=120A,$ $di/dt = 100A/\mu s,$ $V_{DD}=20V, T_j=150^\circ C$ (see Figure 20)		75		ns
$Q_{rr}$	Reverse recovery charge			185		nC
$I_{RRM}$	Reverse recovery current			5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

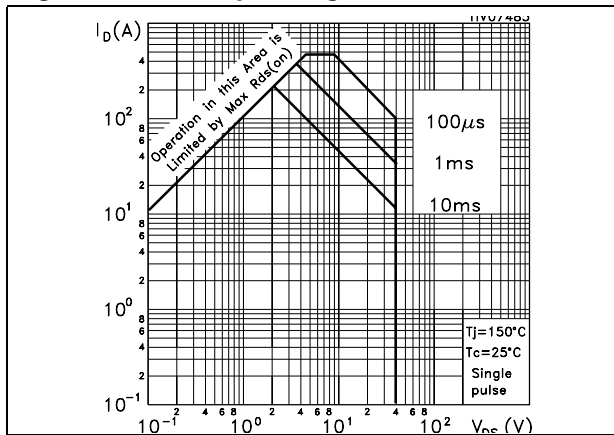


Figure 2. Thermal impedance

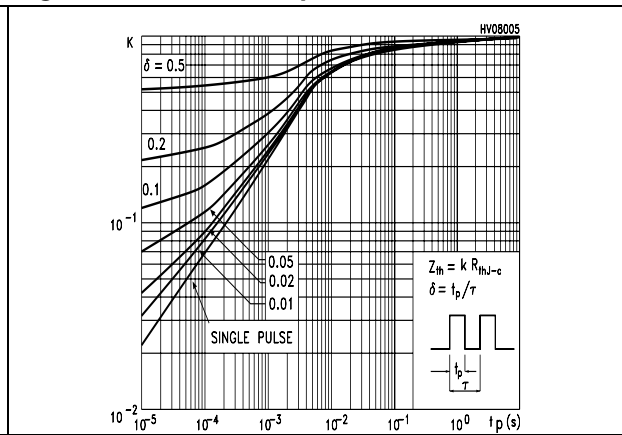


Figure 3. Output characteristics

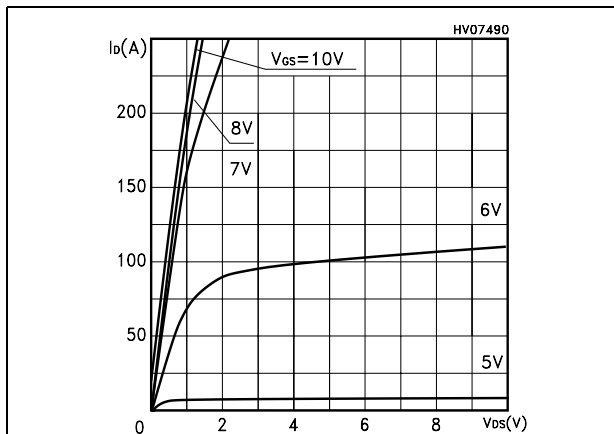


Figure 4. Transfer characteristics

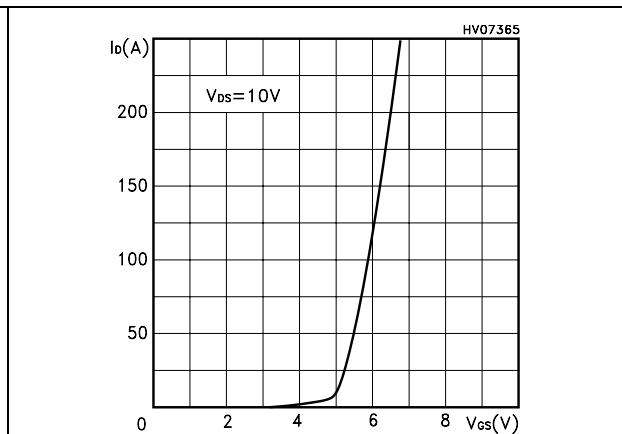


Figure 5. Transconductance

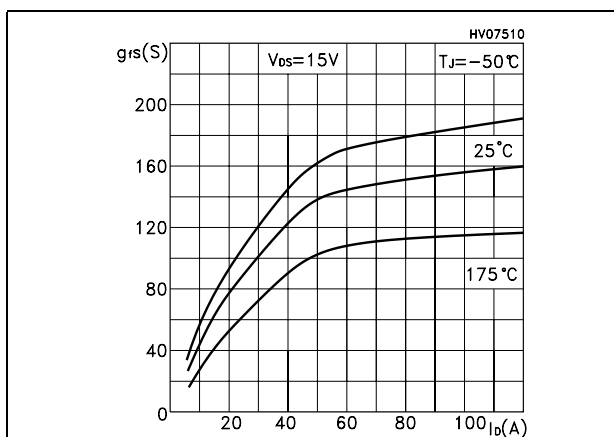


Figure 6. Static drain-source on resistance

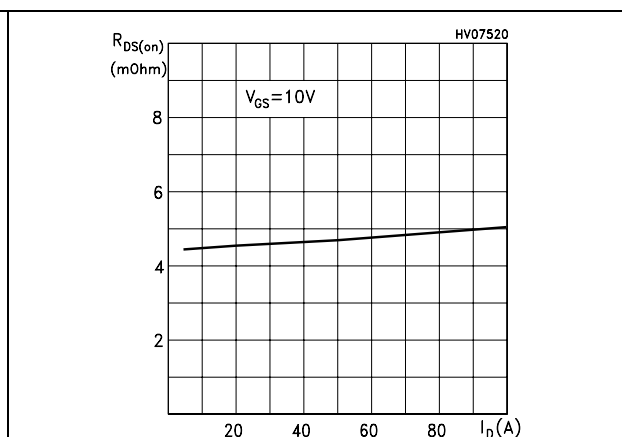


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variation

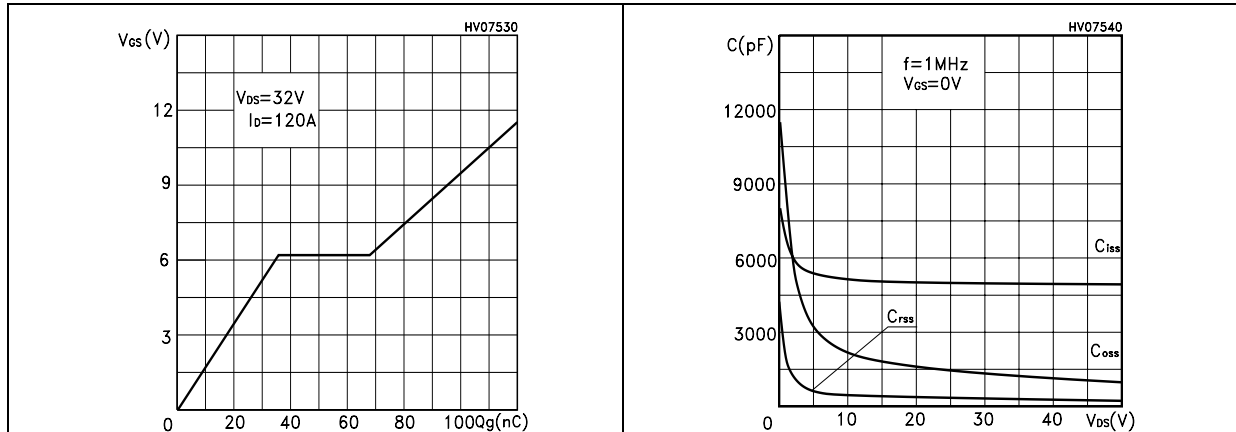


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized  $B_{V_{DS}}$  vs temperature

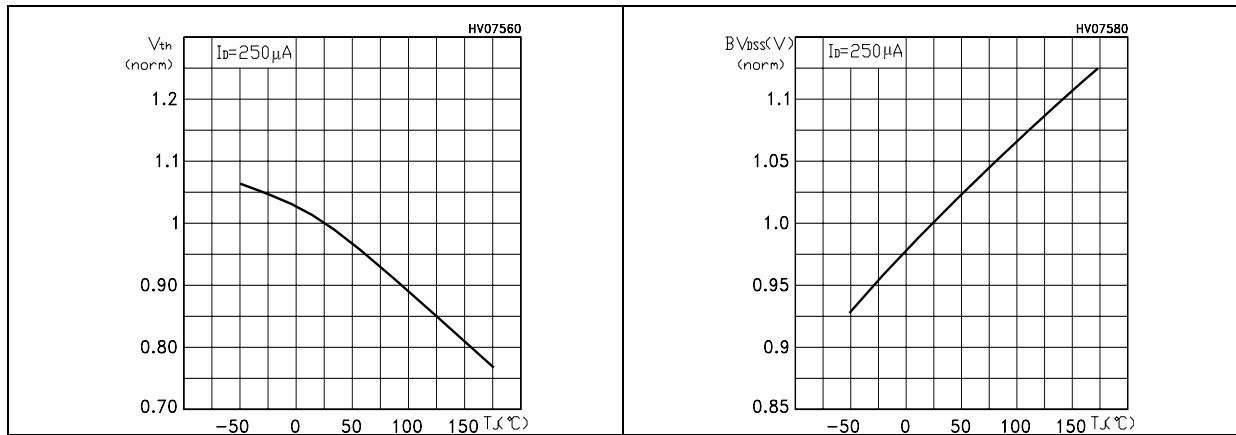


Figure 11. Normalized on resistance vs temperature Figure 12. Source-drain diode forward characteristics

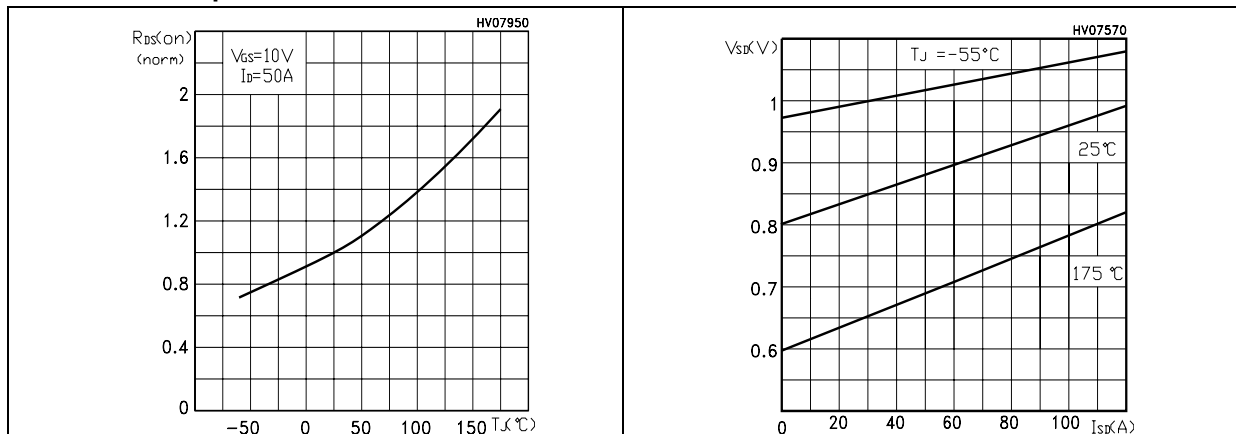


Figure 13. Power derating vs Tc

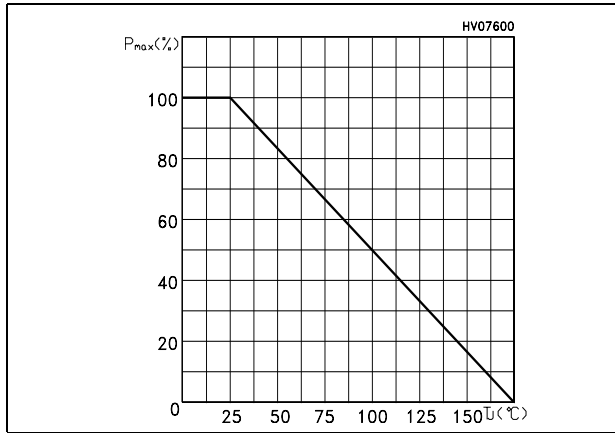


Figure 14. Thermal resistance Rthj-a vs PCB copper area

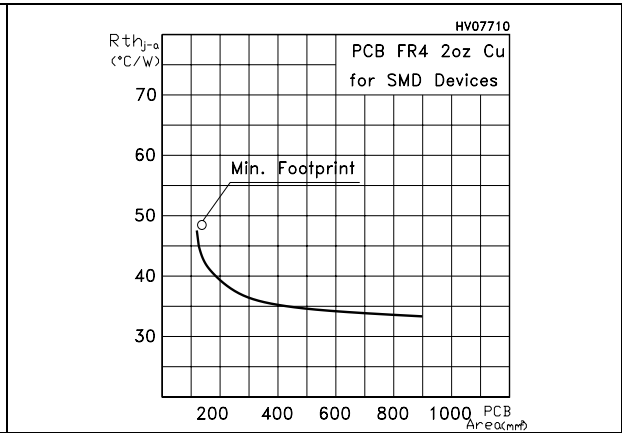


Figure 15. Max id current vs Tc

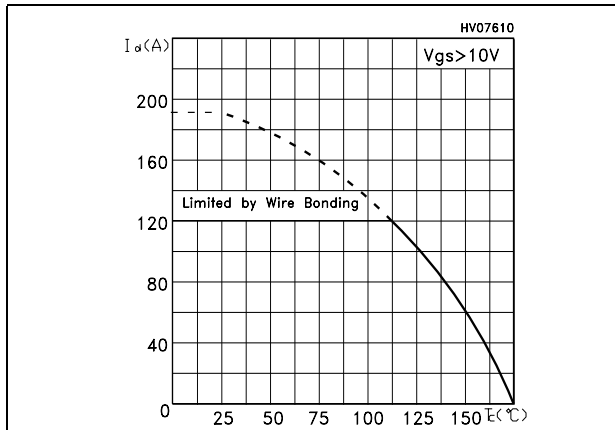


Figure 16. Max power dissipation vs PCB copper area

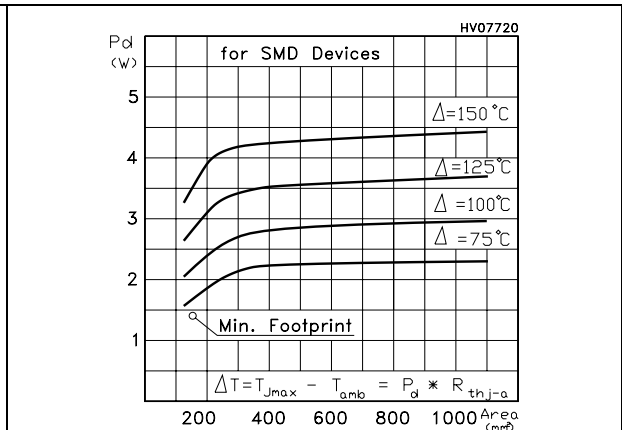
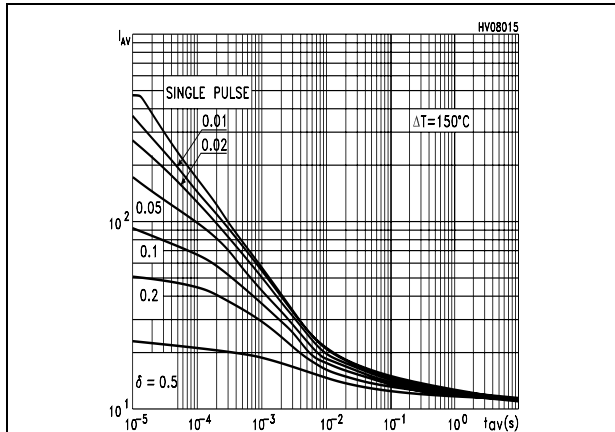




Figure 17. Allowable I<sub>AV</sub> vs time in avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * BV_{DSS} * I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

I<sub>AV</sub> is the allowable current in avalanche

P<sub>D(AVE)</sub> is the average power dissipation in avalanche (single pulse)

t<sub>AV</sub> is the time in avalanche

To derate above 25 °C, at fixed I<sub>AV</sub>, the following equation must be applied:

$$I_{AV} = 2 * (T_{jmax} - T_{CASE}) / (1.3 * BV_{DSS} * Z_{th})$$

Where:

Z<sub>th</sub> = K \* R<sub>th</sub> is the value coming from Normalized Thermal Response at fixed pulse width equal to T<sub>AV</sub>.

### 3 Test circuit

Figure 18. Switching times test circuit for resistive load

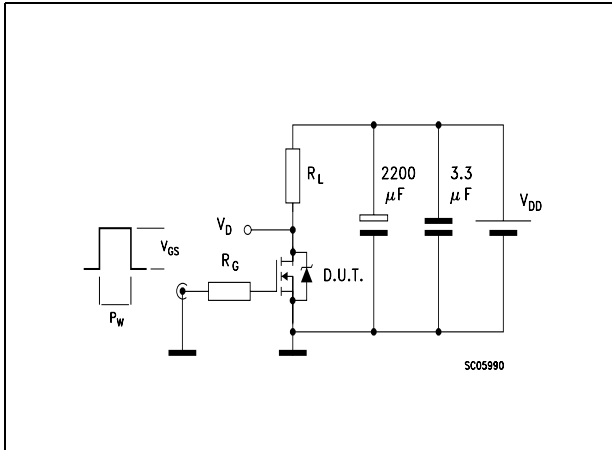


Figure 19. Gate charge test circuit

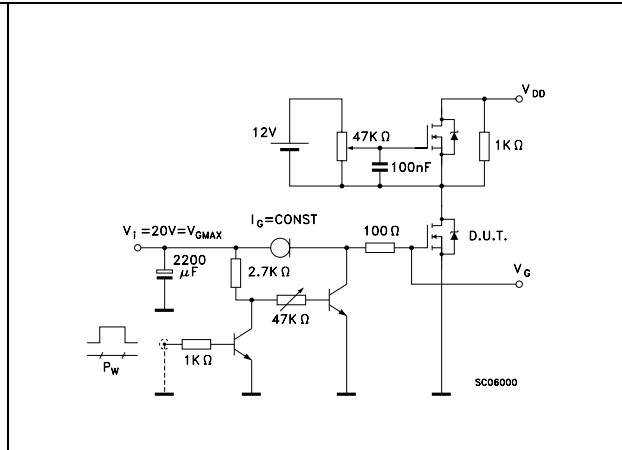


Figure 20. Test circuit for inductive load switching and diode recovery times

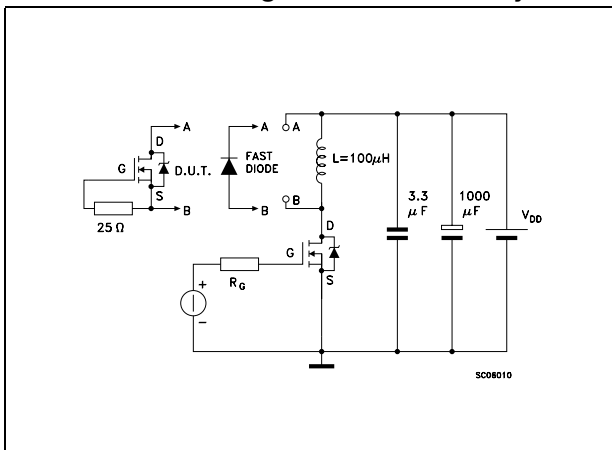


Figure 21. Unclamped Inductive load test circuit

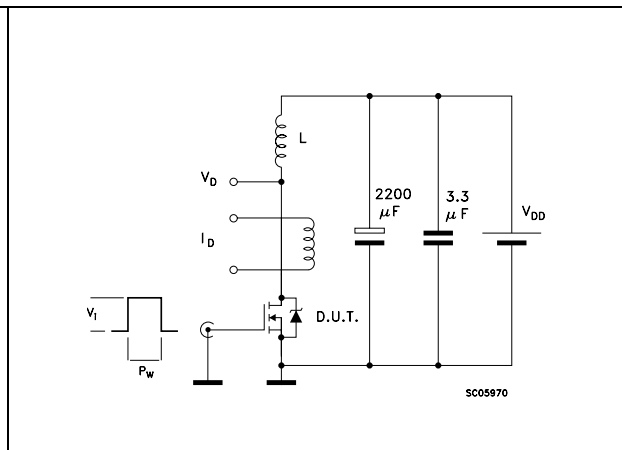


Figure 22. Unclamped inductive waveform

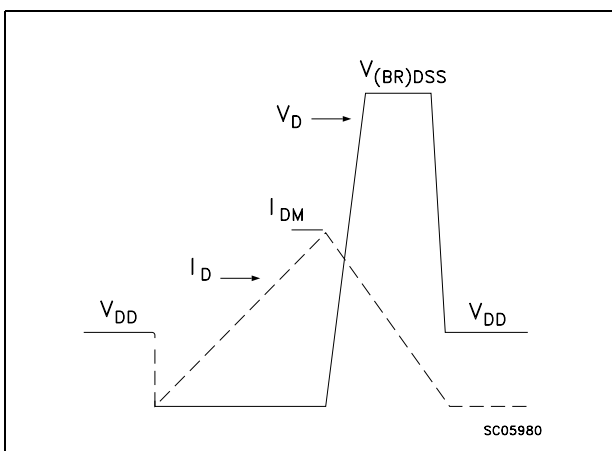
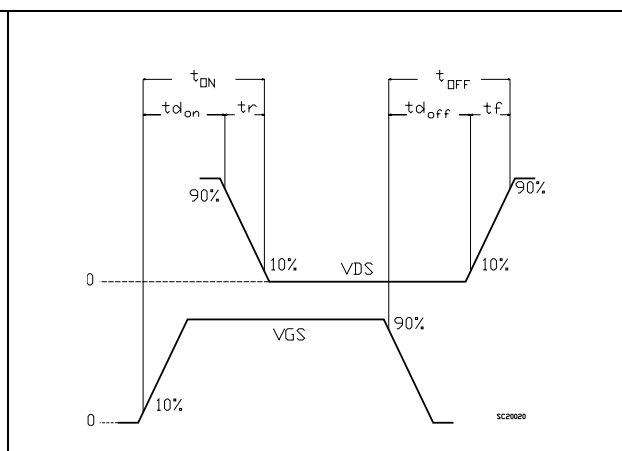


Figure 23. Switching time waveform

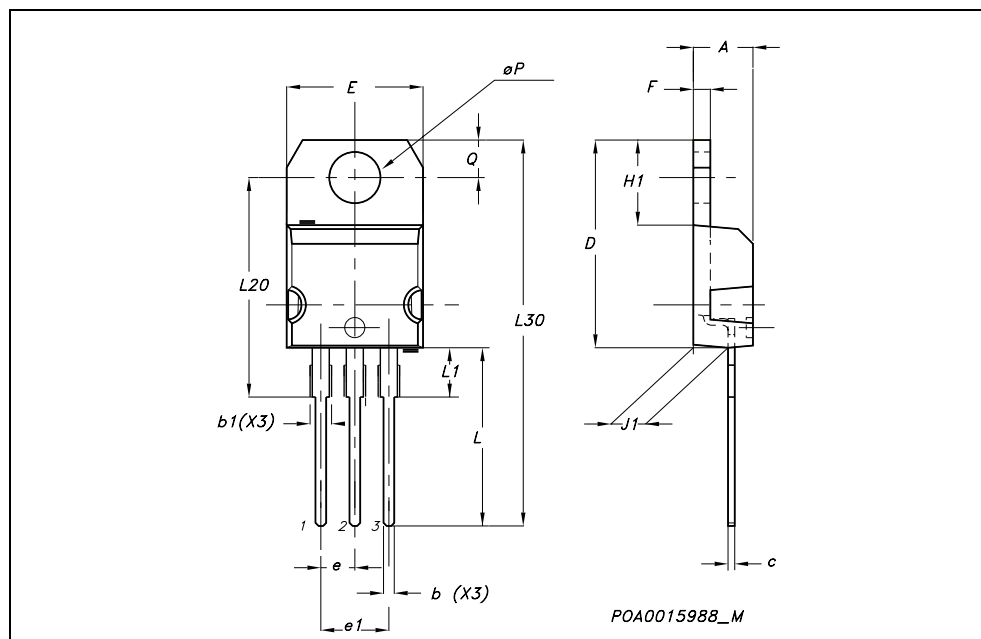


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



## 5 Revision history

**Table 6. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
28-Feb-2005	1	First release.
02-Oct-2006	2	New template, no content change

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