STK40N2LLH5

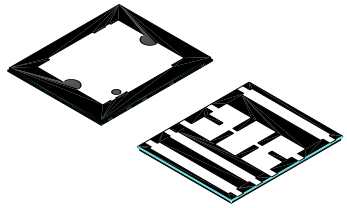
N-channel 25 V, 0.0014 Ω, 40 A, PolarPAK® STripFET™ V Power MOSFET

Preliminary Data

Features

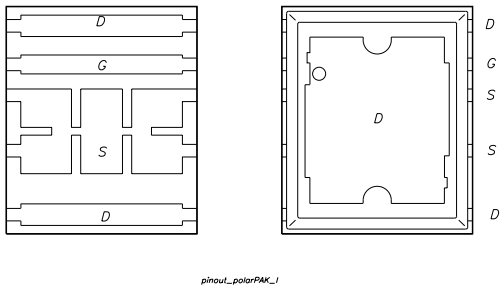
Type	V_{DSS}	$R_{DS(on)}$ max	$R_{DS(on)}$*Q_g	P_{TOT}
STK40N2LLH5	25V	<0.0017Ω	61.2nC*mΩ	5.2W

- Ultra low top and bottom junction to case thermal resistance
- Extremely low on-resistance $R_{DS(on)}$
- $R_{DS(on)}$*Q_g industry benchmark
- High avalanche ruggedness
- Fully encapsulated die
- 100% Matte tin finish (in compliance with the 2002/95/EC european directive)
- PolarPAK® is a trademark of VISHAY



PolarPAK®

Figure 1. Internal schematic diagram



Bottom View **Top View**

Application

- Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET™ technology. The lowest available $R_{DS(on)}$*Q_g, in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

Table 1. Device summary

Order code	Marking	Package	Packaging
STK40N2LLH5	402L5	PolarPAK®	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	25	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	40	A
I_D	Drain current (continuous) at T_C = 100 °C	25	A
I_{DM} (2)	Drain current (pulsed)	160	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	5.2	W
	Derating factor	0.0416	W/°C
E_{AS} (3)	Single pulse avalanche energy	TBD	J
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. When mounted on FR-4 board of 1inch^2, 2 oz. Cu. and ≤ 10sec
2. Pulse width limited by package
3. Starting T_J = 25 °C, I_D = 20 A, V_{DD} = 25 V

Table 3. Thermal data

Symbol	Parameter	Typ.	Max.	Unit
Rthj-amb(1)	Thermal resistance junction-amb	20	24	°C/W
Rthj-c(2)	Thermal resistance junction-case (top drain)	0.8	1	°C/W
Rthj-c(3)	Thermal resistance junction-case (source)	2.2	2.7	°C/W

1. When mounted on FR-4 board of 1inch^2, 2 oz. Cu. and ≤ 10sec
2. Steady State
3. Measured at Source pin when the device is mounted on FR-4 board in steady state

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	25			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc=125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 20 A V_{GS}= 4.5 V, I_D= 20A		0.0014 0.0018	0.0017 0.0022	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0		4617 1065 170		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 40 A V_{GS} =4.5 V *(see Figure 3)*		34 TBD TBD		nC nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain		TBD		Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}= 15 V, I_D= 20 A, R_G=4.7 Ω, V_{GS}=4.5 V *(see Figure 2)*		TBD TBD		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time			TBD TBD		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				40 160	A A
V_{SD} (2)	Forward on voltage	I_{SD}= 20 A, V_{GS}=0			1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 40 A, di/dt = 100 A/µs, V_{DD}=20 V, T_J=150°C *(see Figure 7)*		TBD TBD TBD		ns nC A

1. Pulse width limited by package
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

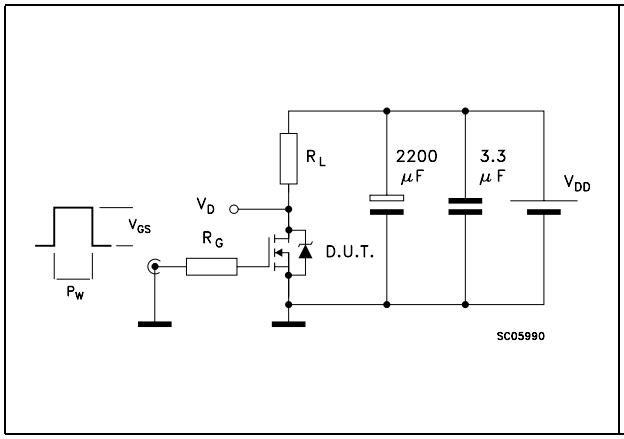


Figure 3. Gate charge test circuit

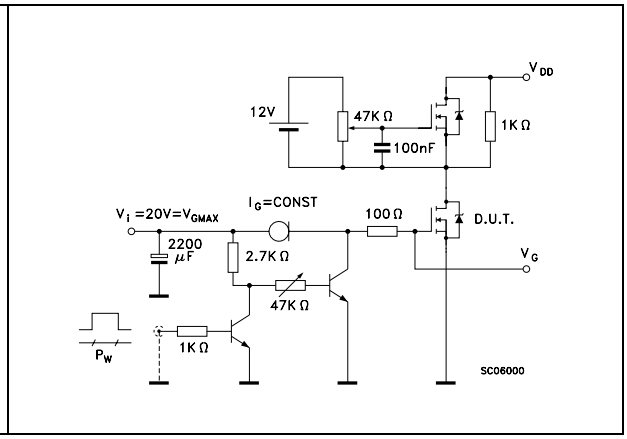


Figure 4. Test circuit for inductive load switching and diode recovery times

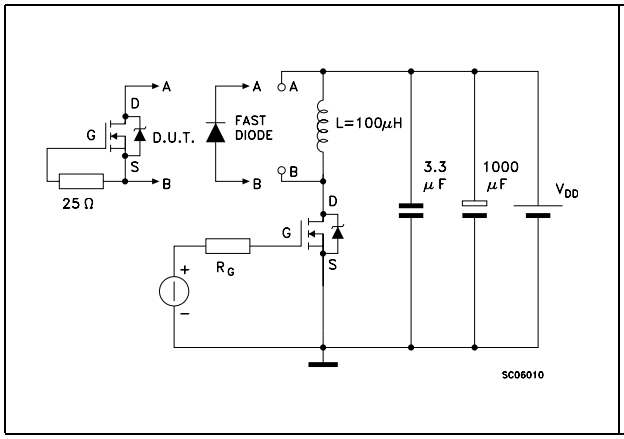


Figure 5. Unclamped inductive load test circuit

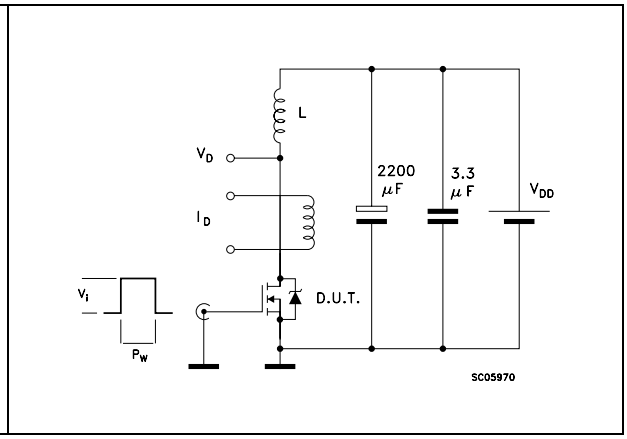


Figure 6. Unclamped inductive waveform

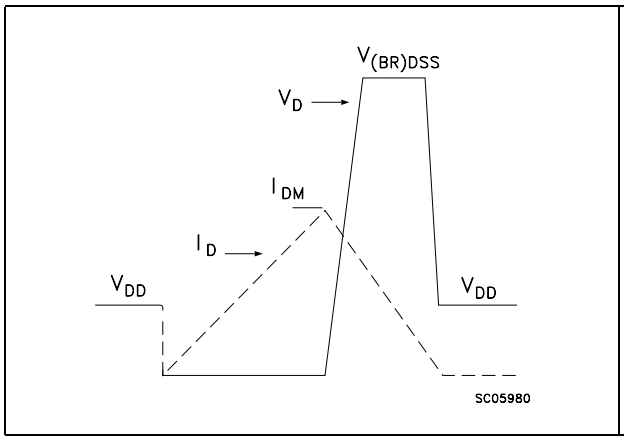


Figure 7. Switching time waveform

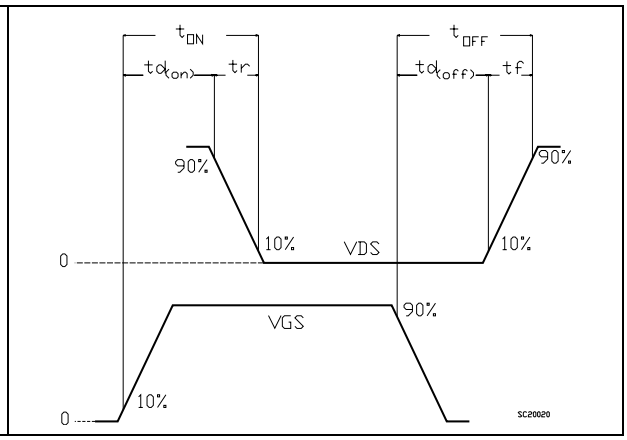
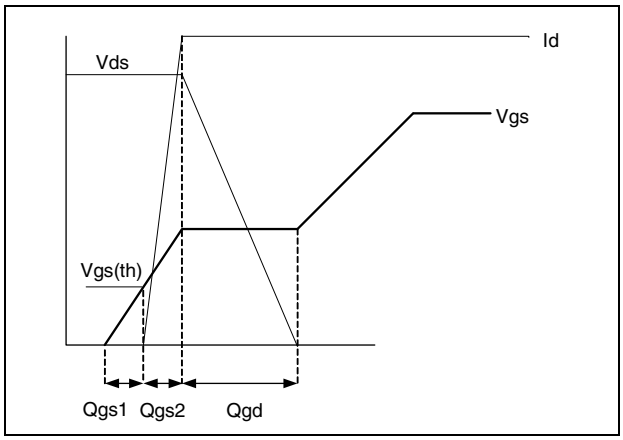


Figure 8. Gate charge waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

Table 8. PolarPAK® (option “L”) mechanical data

Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1			0.05			0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23			0.009		
H2	0.45		0.56	0.018		0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45		0.56	0.018		0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.08	1.13	1.18	0.043	0.044	0.046
K3	1.37			0.054		
K4	0.24			0.009		
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22			0.009		
M4	0.05			0.002		
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20			0.047		
T4	3.90			0.154		
T5		0.18	0.36		0.007	0.014
<	0°	10°	12°	0°	10°	12°

Figure 9. PolarPAK® (option "L") drawings

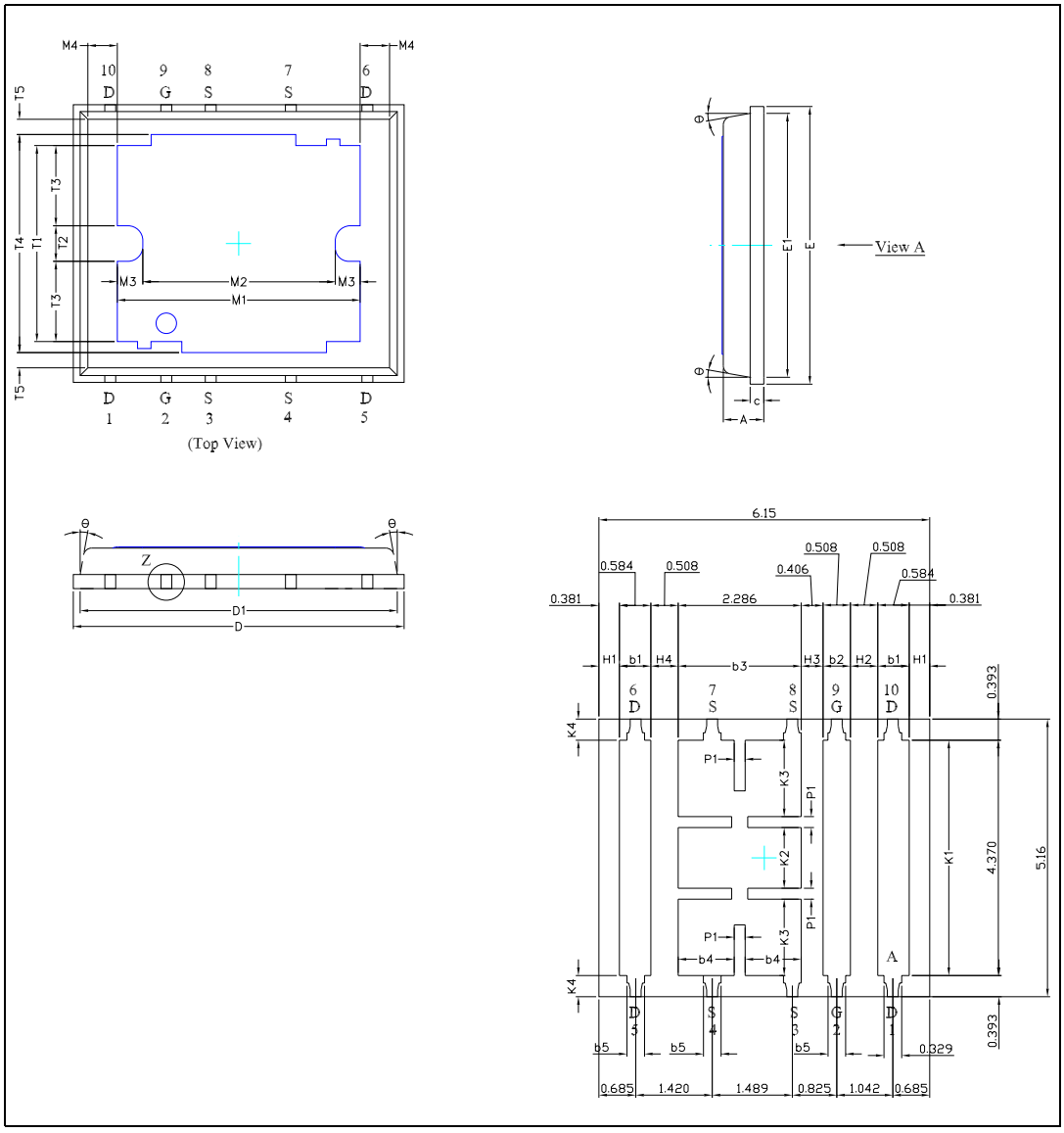
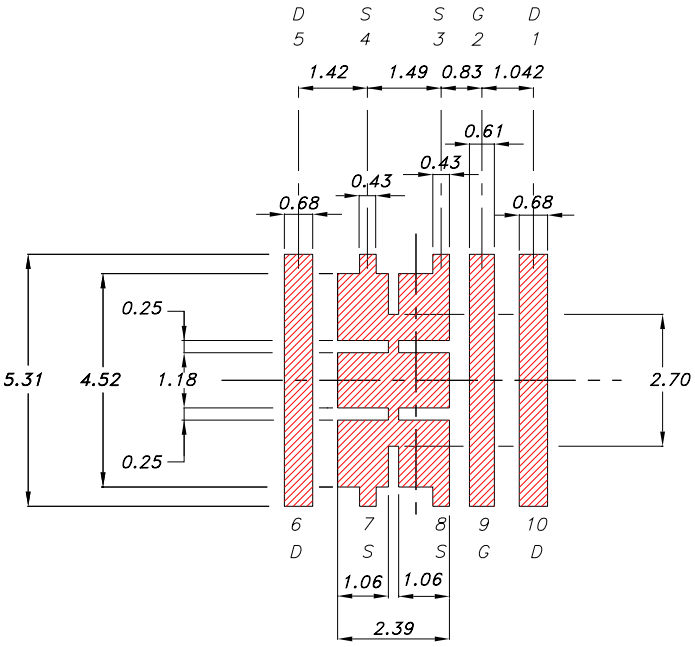


Figure 10. Recommended PAD layout



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Jul-2008	1	First release

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