STD45NF75

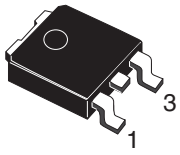
N-channel 75V - 0.018Ω - 40A - DPAK
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STD45NF75	75V	<0.024Ω	40A(1)

1. Current limited by package

- 100% avalanche tested
- Gate charge minimized

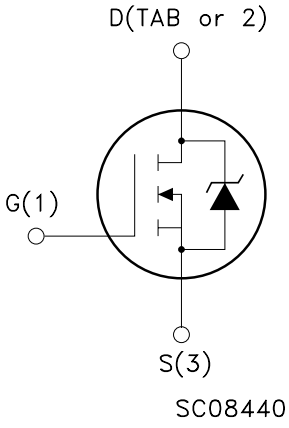


DPAK

Description

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STD45NF75T4	D45NF75	DPAK	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	75	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	75	V
V_{GS}	Gate- source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25°C	40	A
I_D	Drain current (continuous) at T_C = 100°C	30	A
I_{DM} (2)	Drain current (pulsed)	160	A
P_{tot}	Total dissipation at T_C = 25°C	100	W
	Derating Factor	0.67	W/°C
dv/dt (3)	Peak diode recovery voltage slope	20	V/ns
E_{AS} (4)	Single pulse avalanche energy	500	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 40A$, di/dt ≤300A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
4. Starting T_j = 25 °C, I_D = 20A, V_{DD} = 40V

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	1.5	°C/W
Rthj-pcb	Thermal resistance junction-pcb max	see *Figure 15.* and *Figure 16.*	°C/W
T_J	Maximum lead temperature for soldering purpose (1)	275	°C

1. for 10 sec. 1.6 mm from case

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	75			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 20A		0.018	0.024	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 25V, I_D = 20A		50		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		1760 360 140		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 37V, I_D = 20A R_G = 4.7Ω V_{GS} = 10V (see *Figure 19*)		15 40 55 12		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 60V, I_D = 40A, V_{GS} = 10V, R_G = 4.7Ω (see *Figure 20*)		60 13 23	80	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				40 160	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 40A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40A, di/dt = 100A/µs, V_{DD} = 30V, T_j = 150°C (see *Figure 21*)		120 410 7.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

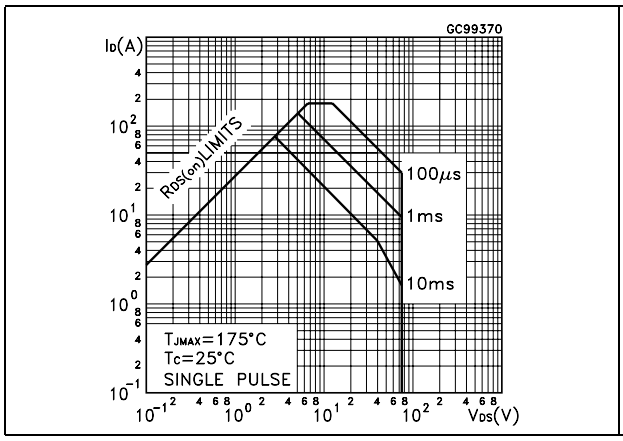


Figure 2. Thermal impedance

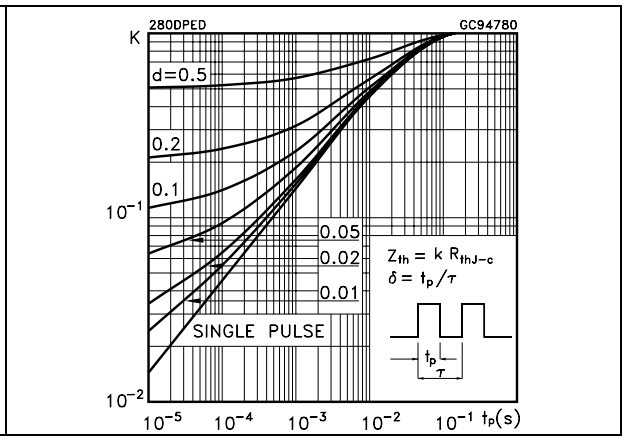


Figure 3. Output characteristics

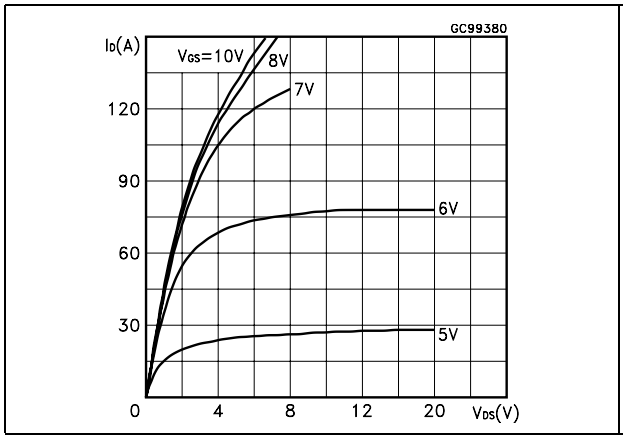


Figure 4. Transfer characteristics

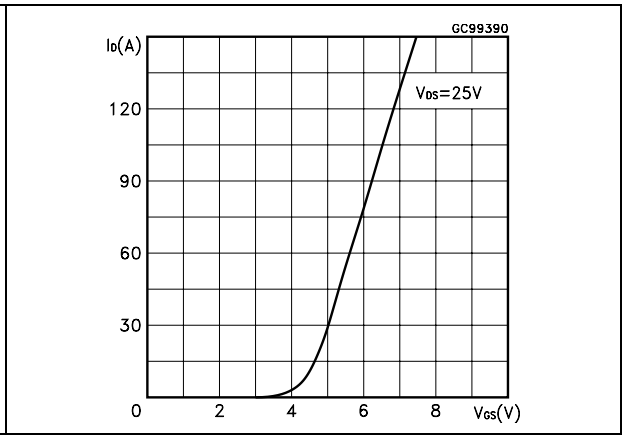


Figure 5. Transconductance

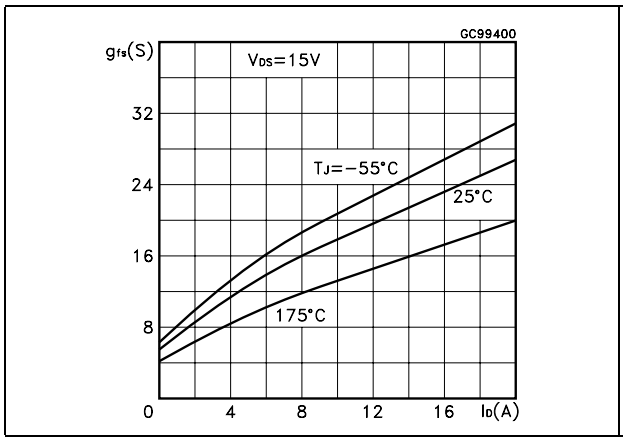


Figure 6. Static drain-source on resistance

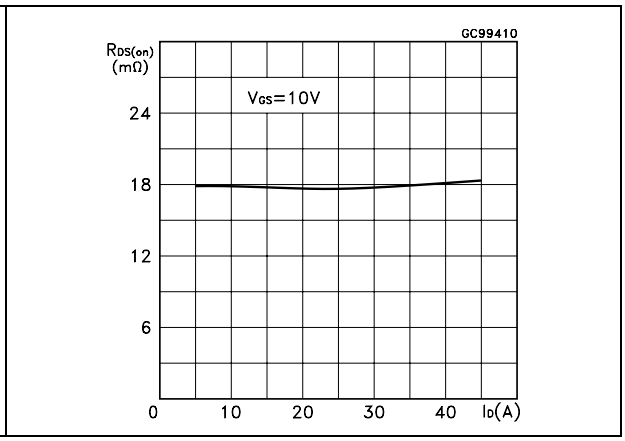


Figure 7. Gate charge vs. gate-source voltage

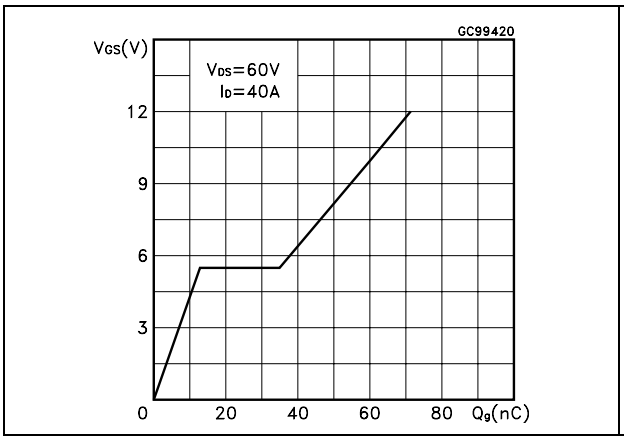


Figure 8. Capacitance variations

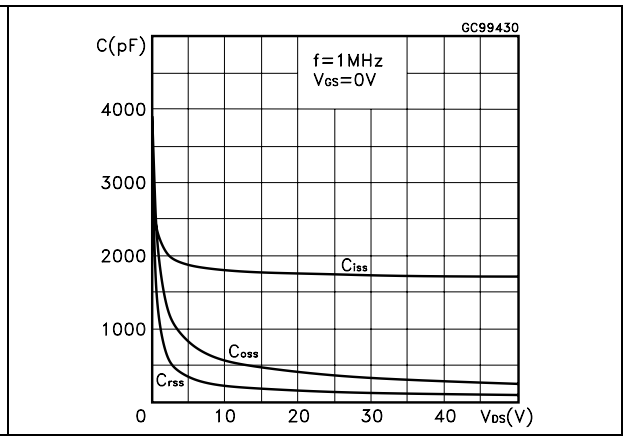


Figure 9. Normalized gate threshold voltage vs. temperature

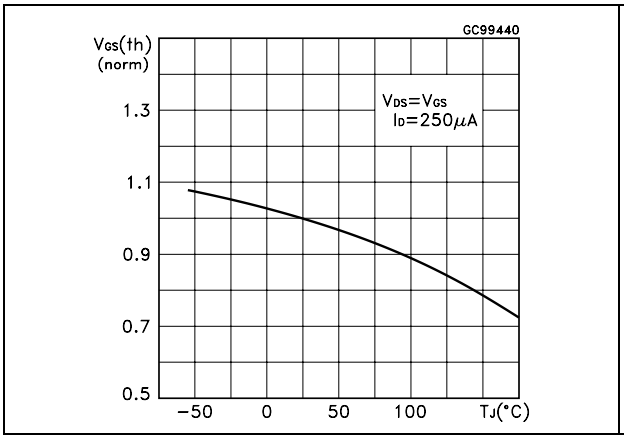


Figure 10. Normalized on resistance vs. temperature

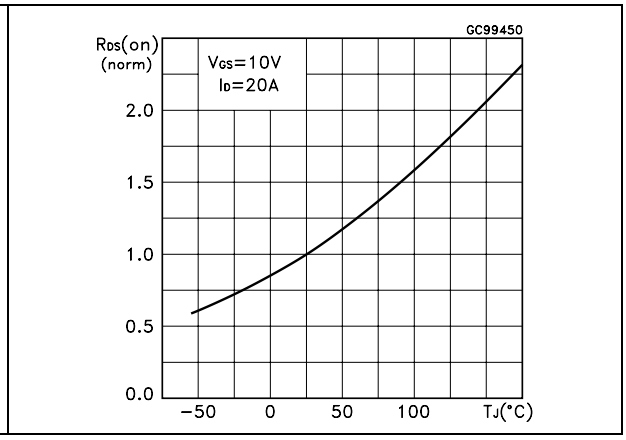


Figure 11. Source-drain diode forward characteristics

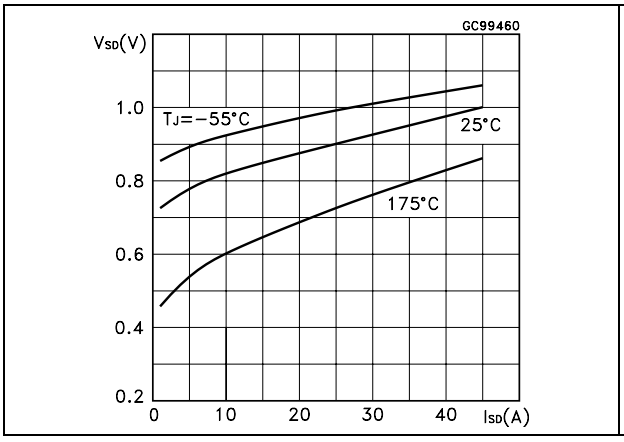


Figure 12. Normalized breakdown voltage vs. temperature

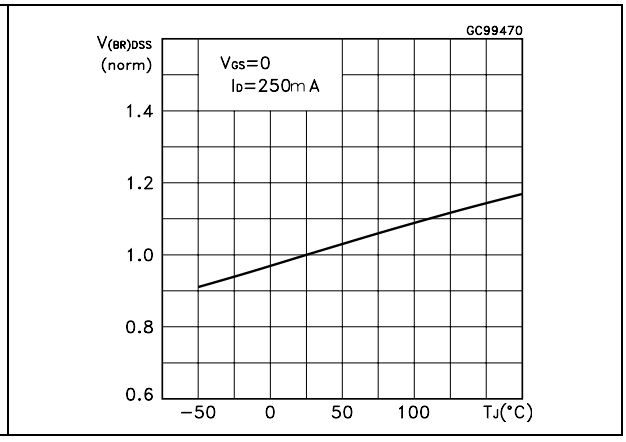


Figure 13. Power derating vs. Tj

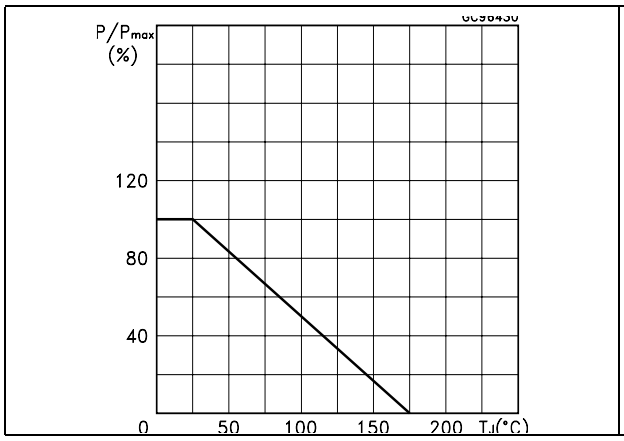


Figure 14. Max Id current vs. Tc

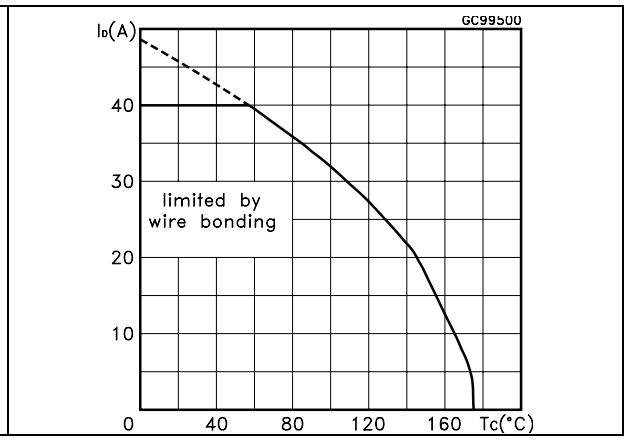


Figure 15. Thermal resistance Rthj-a vs. pcb copper area

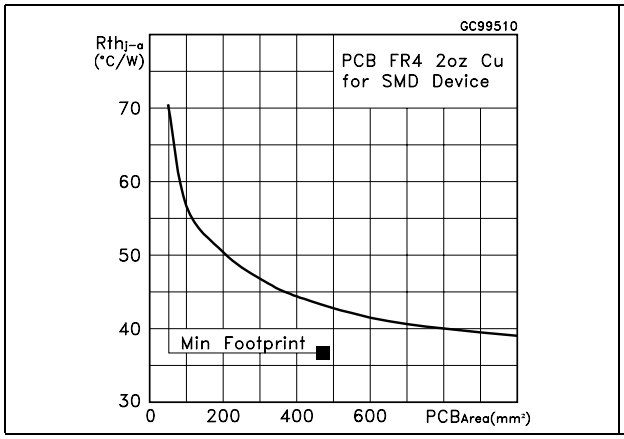


Figure 16. Max power dissipation vs. pcb copper area

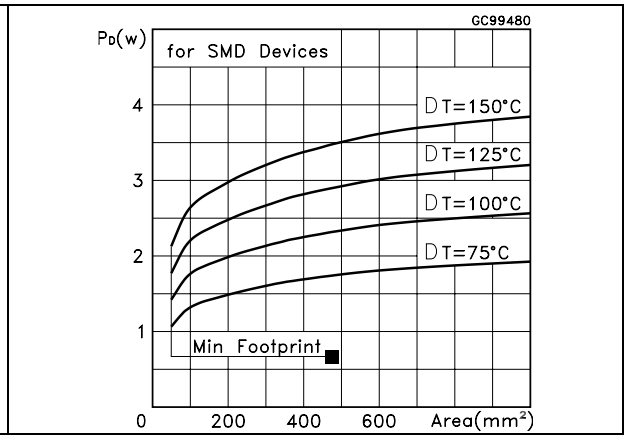
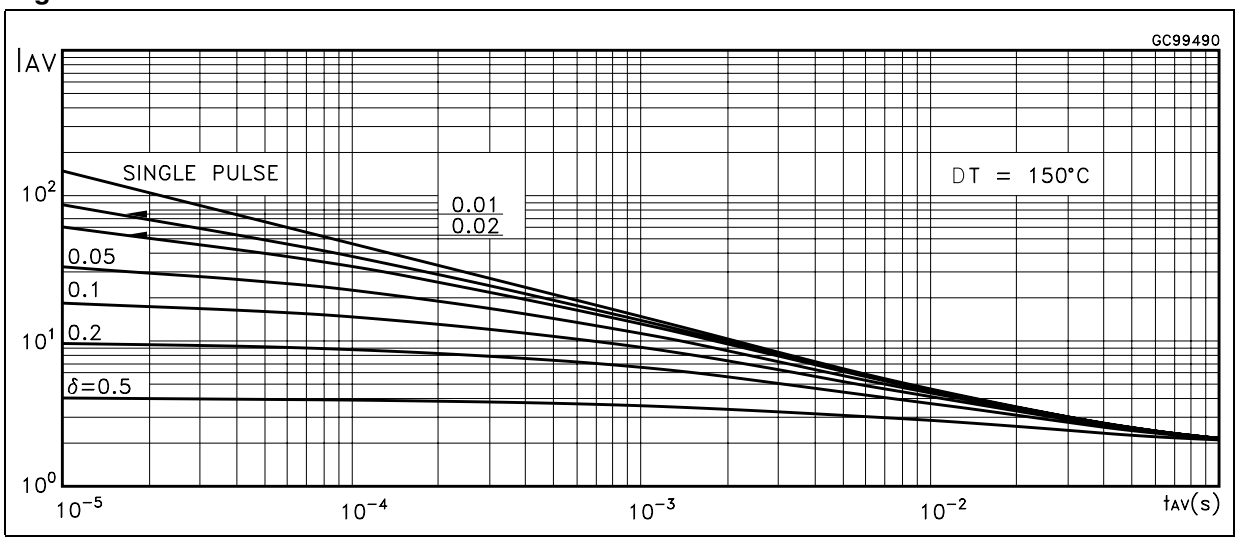


Figure 17. Allowable Iav vs. time in avalanche



The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$P_{D(AVE)} = 0.5 * (1.3 * B_{VDSS} * I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

To de rate above 25 °C, at fixed I_{AV}, the following equation must be applied:

$I_{AV} = 2 * (T_{jmax} - T_{CASE})/ (1.3 * B_{VDSS} * Z_{th})$

Where:

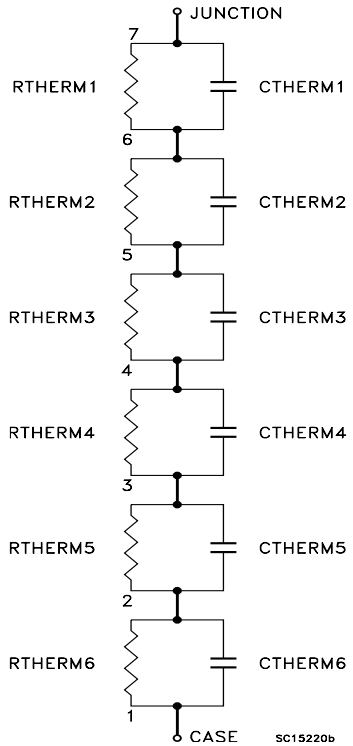
$Z_{th} = K * R_{th}$ is the value coming from normalized thermal response at fixed pulse width equal to T_{AV}.

3 Spice thermal model

Table 6. Spice parameter

Parameter	Node	Value
CTHERM1	7 - 6	$6 * 10^{-4}$
CTHERM2	6 - 5	$8 * 10^{-3}$
CTHERM3	5 - 4	$2 * 10^{-2}$
CTHERM4	4 - 3	$6 * 10^{-2}$
CTHERM5	3 - 2	$9.65 * 10^{-2}$
CTHERM6	2 - 1	$6 * 10^{-1}$
RTHERM1	7 - 6	0.045
RTHERM2	6 - 5	0.105
RTHERM3	5 - 4	0.150
RTHERM4	4 - 3	0.225
RTHERM5	3 - 2	0.375
RTHERM6	2 - 1	0.600

Figure 18.



4 Test circuit

Figure 19. Switching times test circuit for resistive load

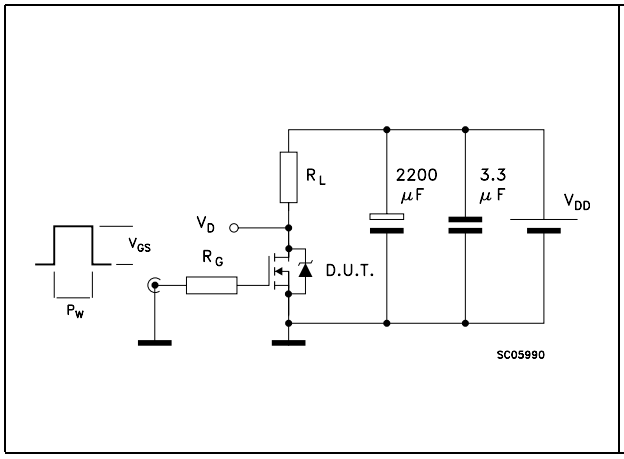


Figure 20. Gate charge test circuit

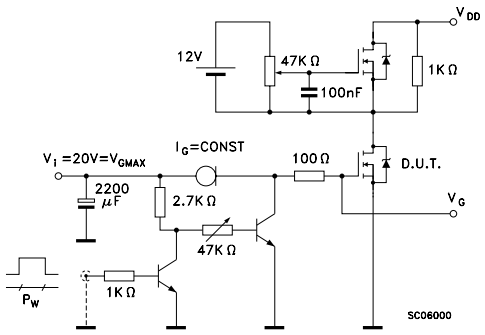


Figure 21. Test circuit for inductive load switching and diode recovery times

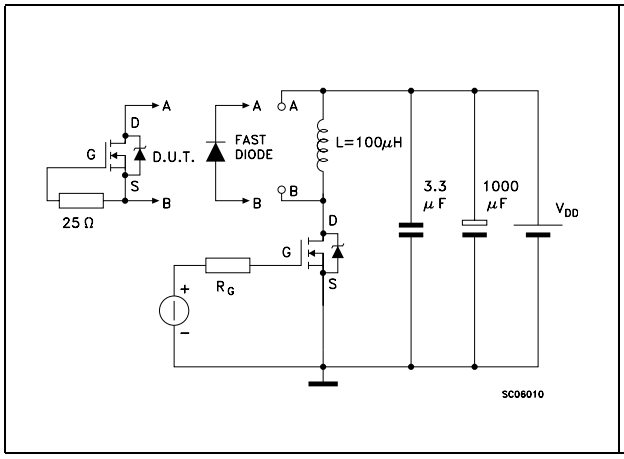


Figure 22. Unclamped Inductive load test circuit

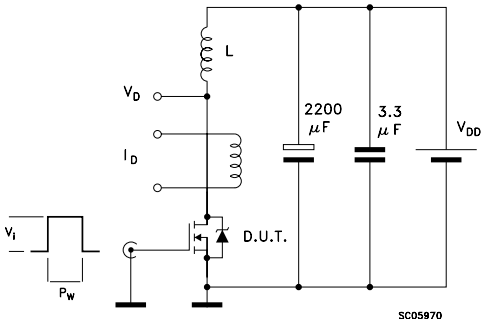


Figure 23. Unclamped inductive waveform

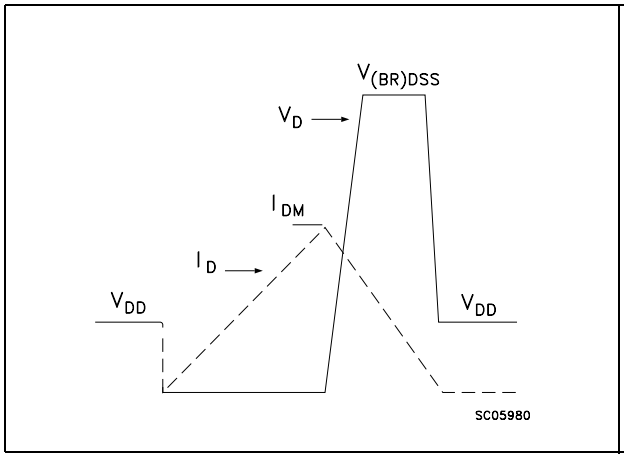
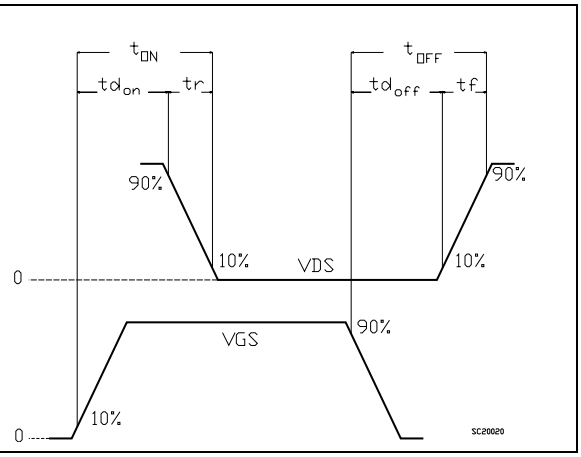


Figure 24. Switching time waveform

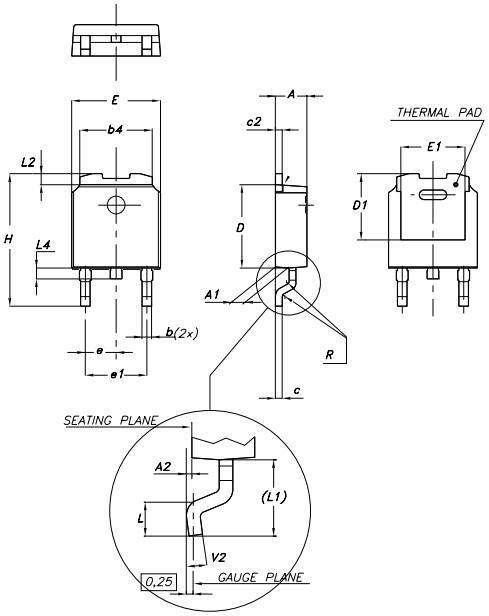


5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



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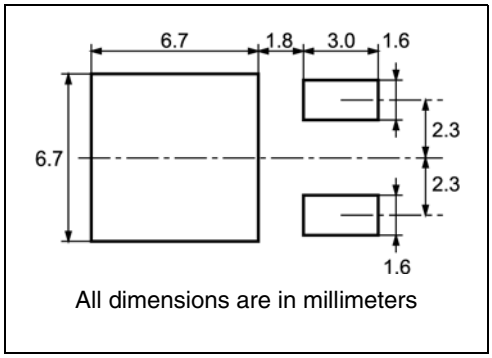
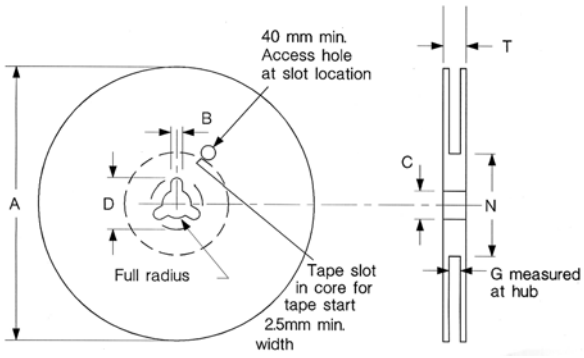
6 Packing mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



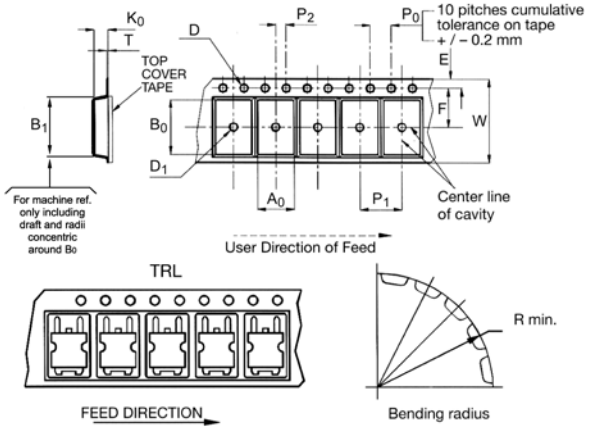
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



7 Revision history

Table 7. Revision history

Date	Revision	Changes
22-Jun-2004	1	Preliminary version
09-Sep-2004	2	Complete version
11-Jul-2006	3	New template, no content change
20-Feb-2007	4	Typo mistake on page 1

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