POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

Customer : _____

Model Type : LCD Module

Sample Code : _____

Mass Production Code : PG9832LRU-ANN-B

Edit : 0

Customer Sign	Sales Sign	Approved By	Prepared By

CONTENTS

1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 98 dots *32 dots
- 1/32 Duty, 1/6 bias
- STN LCD positive, yellow green
- Transflective LCD
- 6 o'clock viewing angle
- 8 bits parallel data input
- Built-in LED backlight

1.2 Mechanical Specifications

- Outline dimension : 52.0mm(L)*44.0mm(W)*13.5mm max.(H)
- Viewing area : 46.0mm *18.5mm
- Active area : 43.08mm *15.64mm
- Dot size : 0.4mm *0.45mm
- Dot pitch : 0.44mm *0.49mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	VDD	-	0	7.0	V
LCD drive Supply voltage	VDD-VEE	-	-	16.5	V
Input voltage	VIN	-	VSS-0.3	0.3	V
Operating temperature	TOPR	-	0	50	°C
Storage temperature	TSTG	-	-20	70	°C
Humidity*1	HD	-	-	90	%RH

1.4 DC Electrical Characteristics

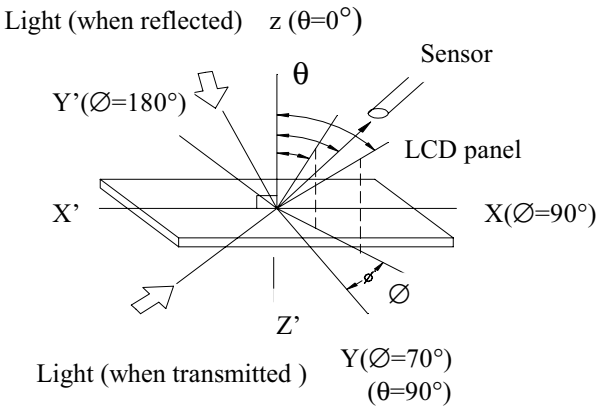
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	VDD	-	4.5	5.0	5.5	V
"H" input voltage	VIH	-	0.8VDD	-	VDD	V
"L" input voltage	VIL	-	VSS	-	0.2VDD	V
Supply current	IOP	VDD=5V	-	1.6	-	mA
LCD driving voltage	VLCD	VDD-VO	-	5.9	-	V

1.5 Optical Characteristics

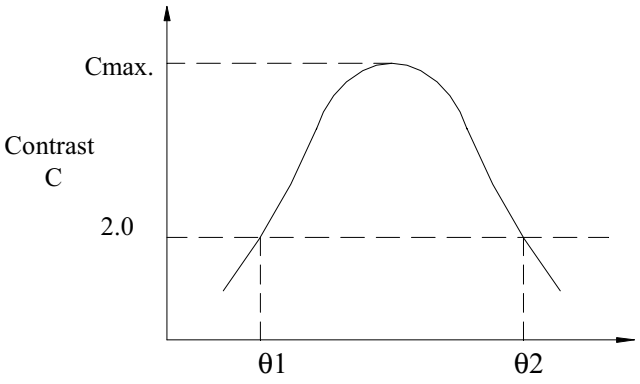
1/32 duty, 1/6 bias, Vopr=5.9, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	C≥2.0,∅=0°C	35°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	-	3	-	Note 3
Response time(rise)	tr	θ=5°, ∅=0°	-	150ms	300ms	Note 4
Response time(fall)	tf	θ=5°, ∅=0°	-	300ms	500ms	Note 4

Note 1: Definition of angles θ and ∅



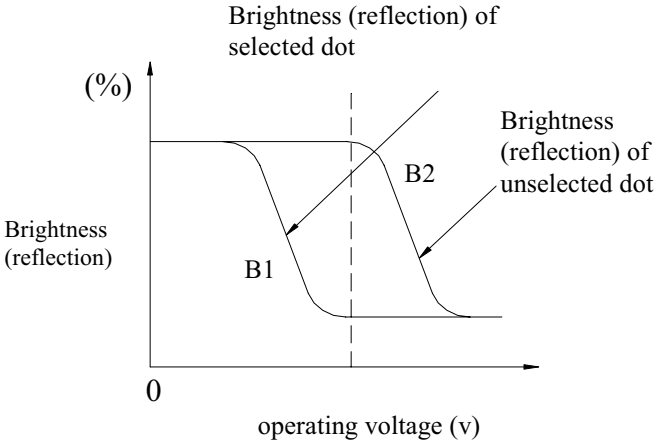
Note 2: Definition of viewing angles θ1 and θ2



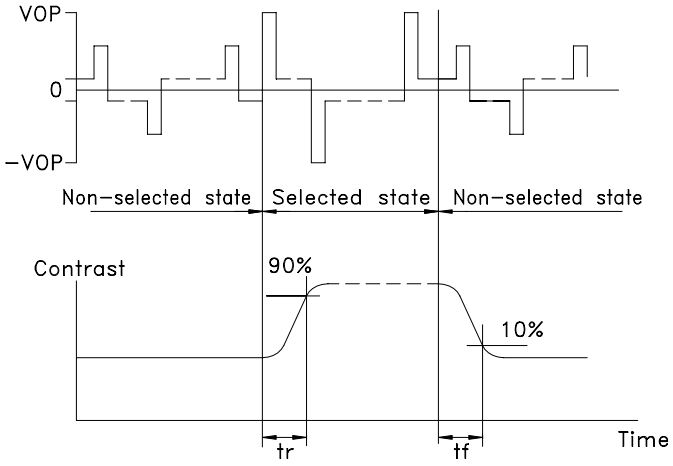
Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltgae f_{FRM} : Frame frequency
t_r : Response time (rise) t_f : Response time (fall)

1.6 Backlight Characteristic

The LCD Module is backlight using a LED panel

- .Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward current	I_F	T_A=25°C	-	300	mA
Reverse voltage	V_R	T_A=25°C	-	8	V
Power dissipation	P_O	T_A=25°C	-	1.38	W
Operating Temperature	T_{OPR}	-	-20	70	°C
Storage temperature	T_{STG}	-	-40	80	°C

- .Electrical Ratings

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	V_F	I_F=120mA	3.8	4.2	4.6	V
Reverse current	I_R	V_R=8V	-	-	0.2	mA
Luminous intensity	I_V	I_F=120mA	200	250	-	cd/m^2
Wavelength	λ p	I_F=120mA	565	-	571	nm
Color	Yellow Green					

2. MODULE STRUCTURE

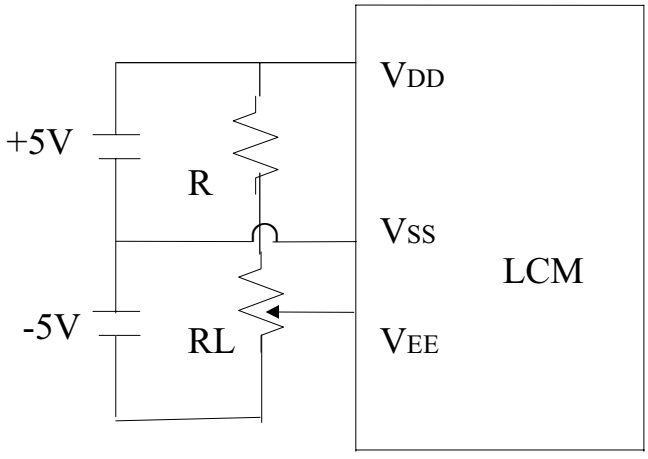
2.1 Counter Drawing

*See Appendix

2.2 Interface Pin Description

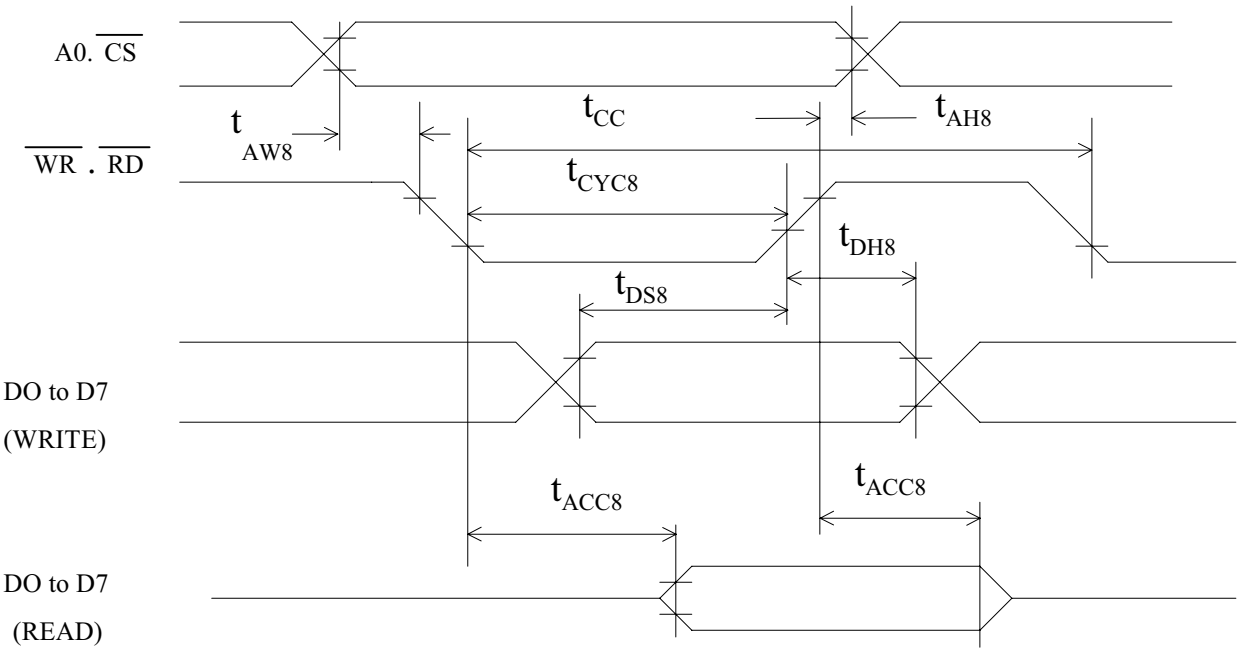
Pin No	Symbol	Function
1	VSS	Signal ground (GND)
2	VDD	Power supply for logic (+5V)
3	VEE	Operating voltage for LCD (variable)
4	A0	"L" is instruction "H" is data
5	$\overline{CS1}$	Chip enable active "L", segment 0~segment 61
6	$\overline{CS2}$	Chip Enable active "L", segment 62~segment 98
7	CL	Clock input 2KHZ
8	$\overline{RD}$ (E)	Data read (68-family MPU : Enable Signal)
9	$\overline{WR}$ (R/ $\overline{W}$)	Data write (68-family MPU : Data read and write)
10-13	DB0~DB3	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. These four are not used during 4-bit operation.
14-17	DB4~DB7	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCD module. DB7 can be used as a busy flag.
18	RES	Reset the system
19	A	LED backlight drive voltage V+
20	K	LED backlight drive voltage ground

Contrast Adjust

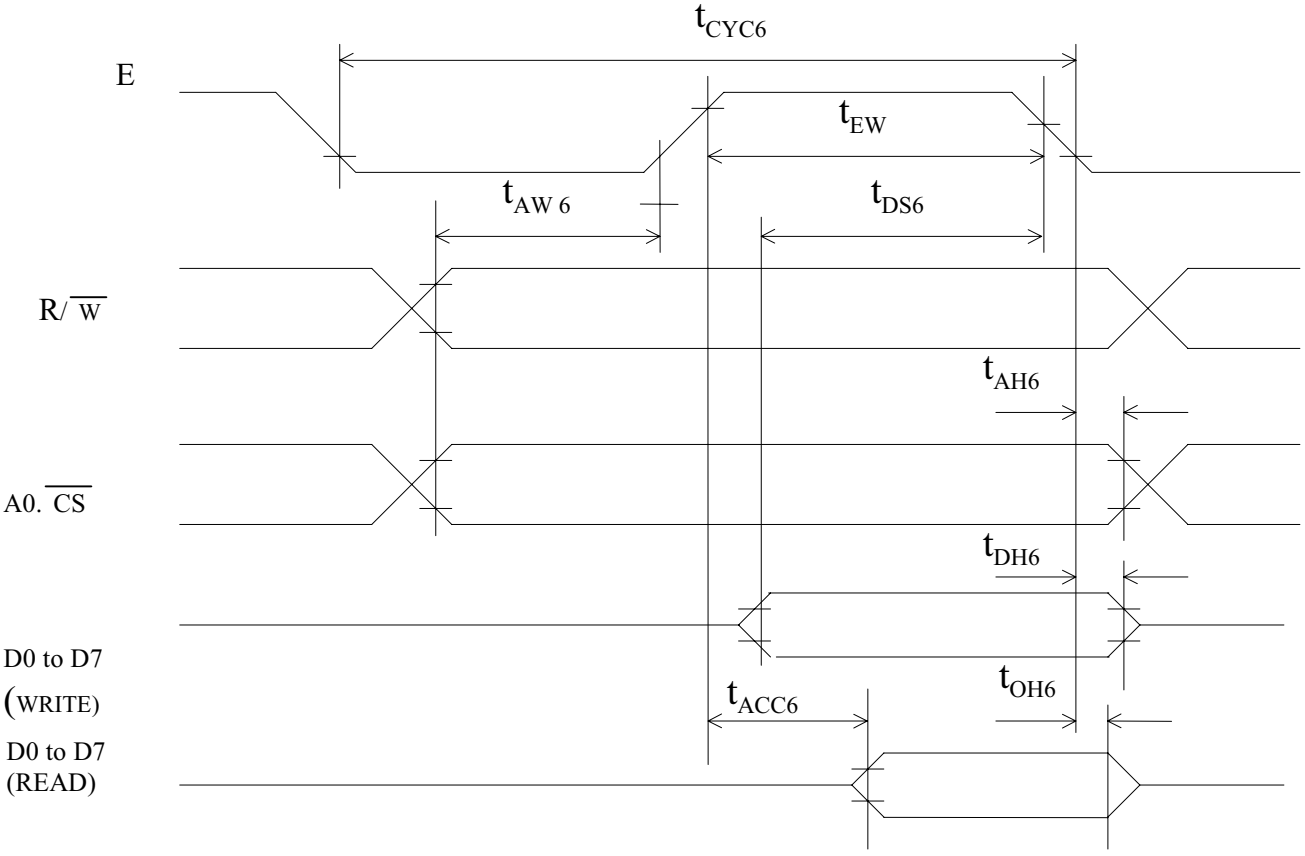


2.3 Timing Characteristics

•.MPU Bus Read/Write I (80-family MPU)



• MPU Bus Read/Write II (68-family MPU)



•MPU Bus Read/Write I (80-family MPU)

V_{DD}=+5V±10%,V_{SS}=0V,Ta=-20 to 70°C

Item	Symbol	Conditions	Min.	Max.	Unit
Address hold time	tAH8	-	10	-	ns
Address setup time	tAW8	-	20	-	ns
System cycle time	tCYC8	-	1000	-	ns
Control pulse width	tCC	-	200	-	ns
Data setup time	tDS8	-	80	-	ns
Data hold time	tDH8	-	10	-	ns
RD access time	tACC8	CL=100 PF	-	90	ns
Output disable time	tCH8		10	60	ns

•MPU Bus Read/Write II (68-family MPU)

V_{DD}=+5V±10% ,V_{SS}=0V,Ta=-20 to 70°C

Item		Symbol	Conditions	Min.	Max.	Unit
System cycle time		tcyc6	-	1000	-	ns
Address setup time		tAW6	-	20	-	ns
Address hold time		tAH6	-	10	-	ns
Data hold time		tDS6	-	80	-	ns
Data hold time		tDH6	-	10	-	ns
Output disable time		tOH6	CL=100 PF	10	60	ns
Access time		tACC6		-	90	ns
Enable pulse width	Read	tEW	-	100	-	ns
	Write		-	80	-	ns

2.4 Display Command

COMMAND

Summary

Command	Code											Function
	A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D5	D2	D1	D0	
Display On/Off	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0:OFF
Display start line	0	1	0	1	1	0	Display start address(o to 31)					Specifies RAM line corresponding to top line of display.
Set page address	0	1	0	1	0	1	1	1	0	Page(o to 3)		Sets display RAM page in page address register.
Set column (segment) address	0	1	0	0	Column address (o to 79)							Sets display RAM column address in column address register.
Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
Write display data	1	1	0	Write data								Write data from data bus into display RAM.
Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1:CCW output
Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1:static drive, 0: Normal driving
Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD duty cycle 1: 1/32, O: 1/16
Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Table 1

Command description

Table 1 is the command table. The SED1520 series identifies a data bus using a combination of A0 and R/$\overline{W}$ (RD or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock). Its speed is very high. The busy check is usually not required.

Display ON/OFF

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	D	AEH,AFH

This command turns the display on and off.
- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown if Figure 1 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command the vertical smooth scrolling and paging can be used.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H,DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 1.

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H,BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

Set column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H,4FH

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

Read Status

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ACD bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-u → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF

ON/OFF=0: Display ON

- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bit of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then
increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH,...(inverted)
D=0: SEG0 ← column address 00H,...(normal)

This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 1 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, ,A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

Select Duty

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, ,A9H

This command sets the duty cycle of the LCD drive.
SED1520
D=1: 1/32 duty cycle
D=0: 1/16 duty cycle

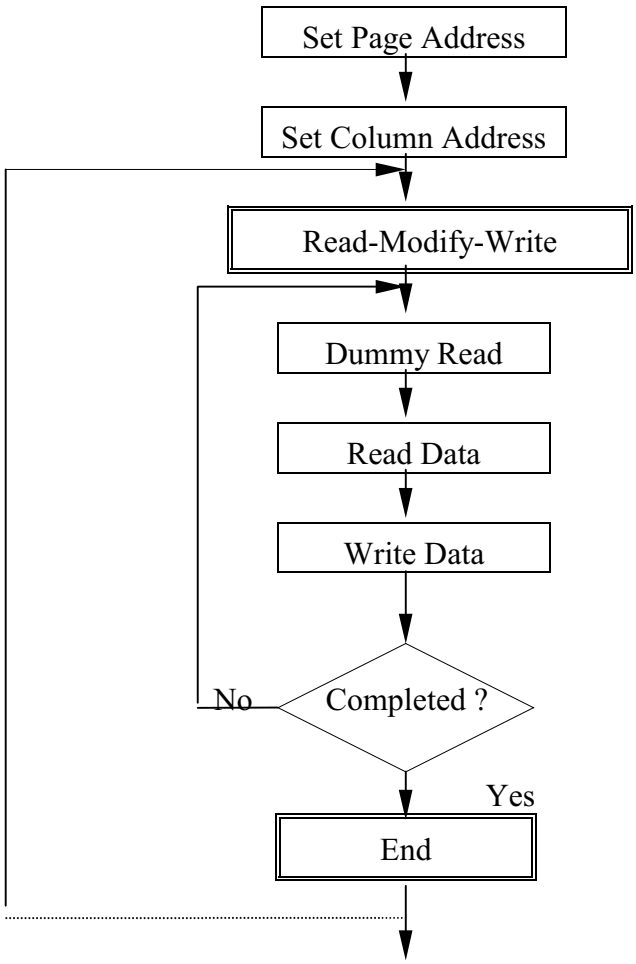
Read-Modify-Write

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	EOH

This command defeats column address register auto-increment after data reads. The current contents of the column address register are saved. This mode remains active until an End command is received.
• Operation sequence during cursor display.

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

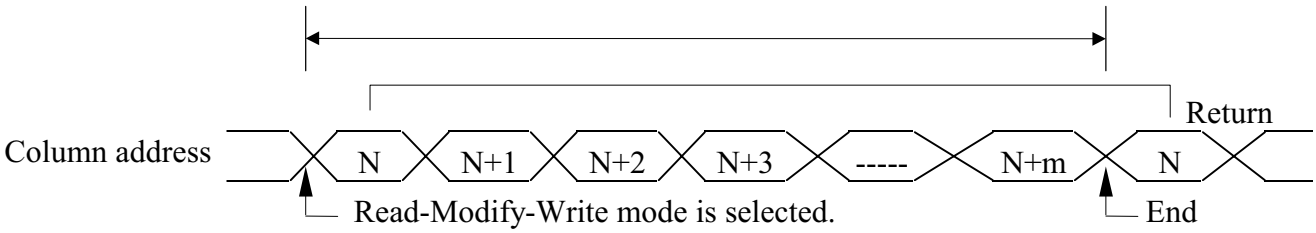
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



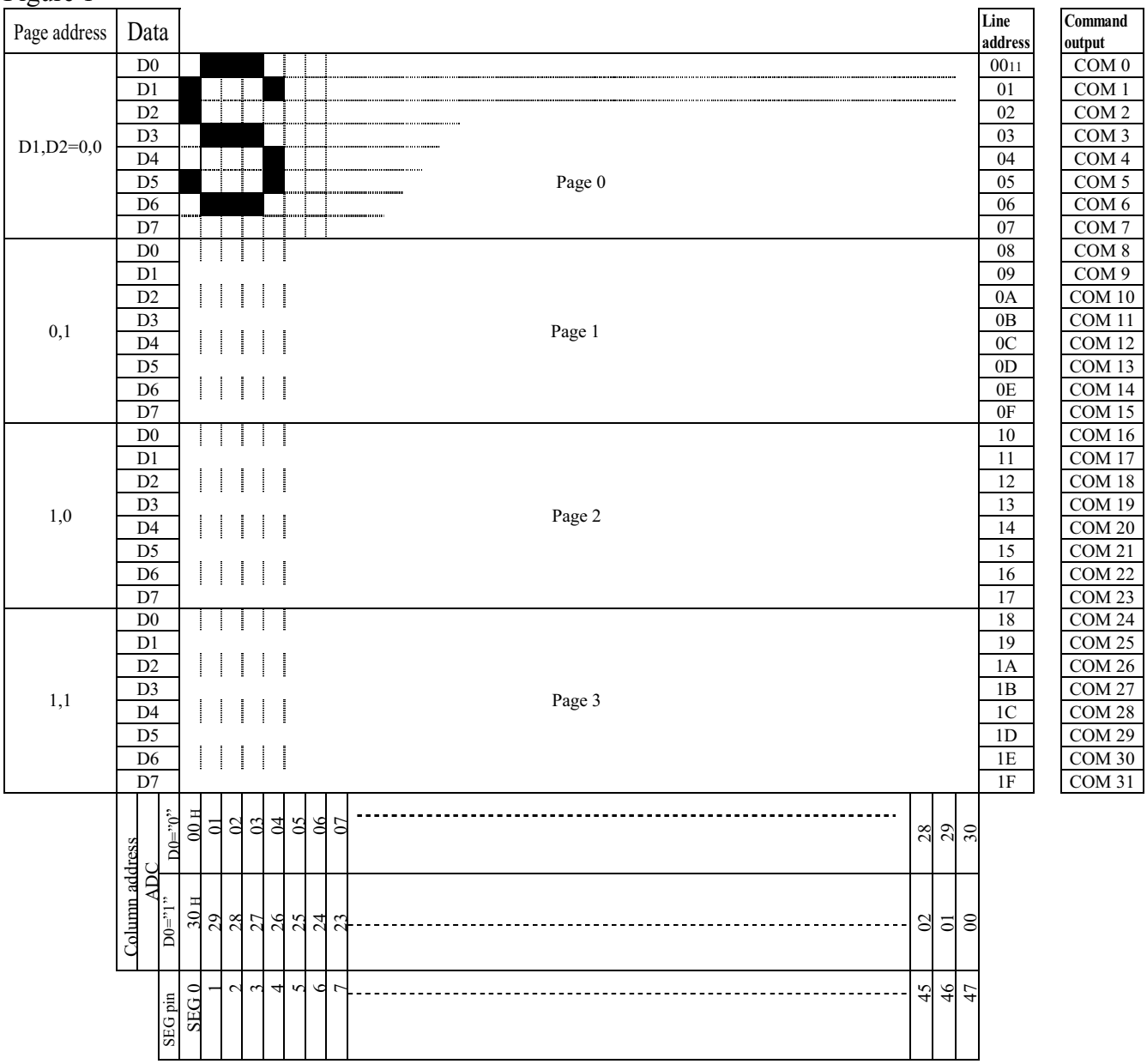
Reset

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears

- the display start line register.
- and set page address register to 3 page.
  It does not affect the contents of the display data RAM.

Figure 1



Display Data RAM Addressing

- (98 * 32) is consisted of 2(49 * 32), $\overline{CS1}$ enable left (49 * 32)
  $\overline{CS2}$ enable right (49 *32)