

POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

Customer : _____

Model Type : LCD Module

Sample Code : _____

Mass Production Code : PG320240LRF-CNN-H-33

Edit : 0

Customer Sign	Sales Sign	Approved By	Prepared By

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1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 320 dots *240 dots
- 1/240 Duty, 1/12 bias
- FSTN LCD, positive
- Transflective LCD
- 6 o'clock viewing angle
- 4 bits parallel data input ,without controller IC
- LED backlight

1.2 Mechanical Specifications

- Outline dimension : 150.5mm(L)*96.8mm(W)*12.2mm max.(H)
- Viewing area : 105.0mm *80.0mm
- Active area : 95.97mm *71.97mm
- Dot size : 0.27mm *0.27mm
- Dot pitch : 0.3mm *0.3mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	VDD	-	-0.3	7.0	V
LCD drive Supply voltage	VDD-VEE	-	-	30.0	V
Input voltage	VIN	-	-0.3	VDD+0.3	V
Operating temperature	TOPR	-	-20	70	°C
Storage temperature	TSTG	-	-30	70	°C
Humidity*1	HD	-	-	90	%RH

1.4 DC Electrical Characteristics

VDD=+5V±10%,VSS=0V,TA=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	VDD	-	4.5	5	5.5	V
“H” input voltage	VIH	-	0.8VDD	-	VDD	V
“L” input voltage	VIL	-	0	-	0.2VDD	V
“H” output voltage	VOH	-	VDD-0.3	-	-	V
“L” output voltage	VOL	-	-	-	0.3	V
Supply current	IDD	VDD=5V	-	-	13	mA
LCD driving voltage	VOP	VDD-VO	-	25.0	28.0	V

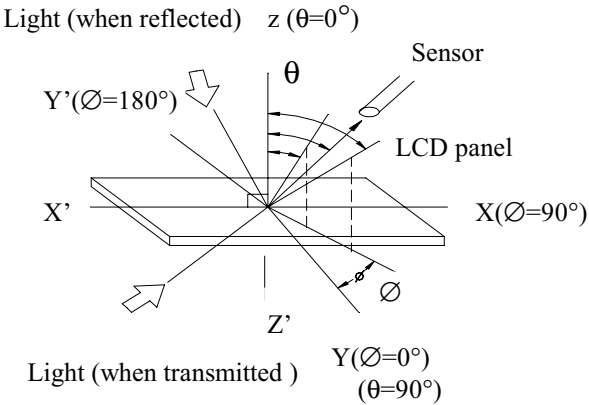


1.5 Optical Characteristics

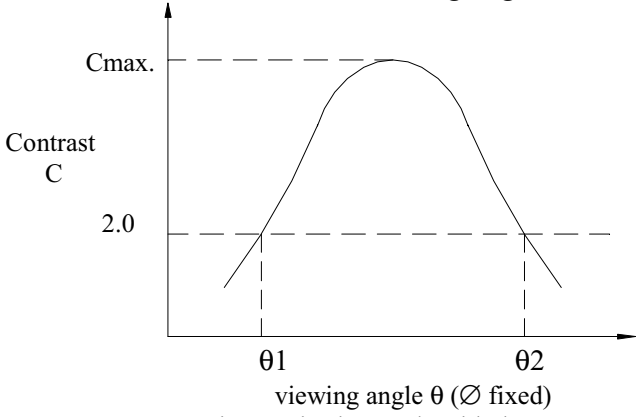
1/240 duty, 1/17 bias, Vopr=25.9V, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	$C \geq 2.0, \varnothing = 0^\circ C$	20°	-	-	Notes 1 & 2
Contrast	C	$\theta = 5^\circ, \varnothing = 0^\circ$	-	5	-	Note 3
Response time(rise)	tr	$\theta = 5^\circ, \varnothing = 0^\circ$	-	190ms	290ms	Note 4
Response time(fall)	tf	$\theta = 5^\circ, \varnothing = 0^\circ$	-	400ms	600ms	Note 4

Note 1: Definition of angles θ and \varnothing



Note 2: Definition of viewing angles θ_1 and θ_2

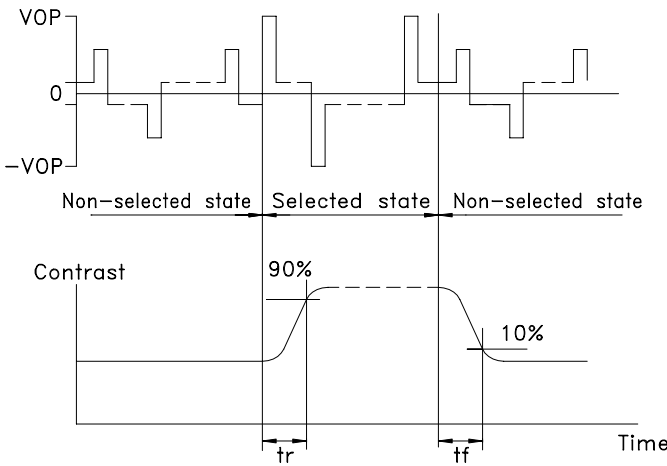
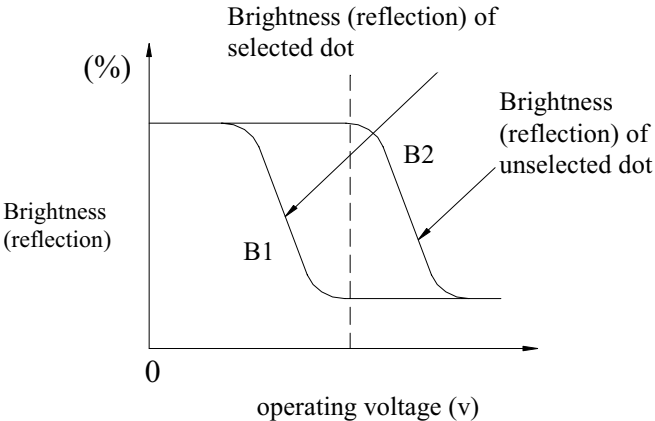


Note : Optimum viewing angle with the naked eye and viewing angle θ at Cmax. Above are not always the same

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$

Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm²

V_{OPR} : Operating voltage f_{FRM} : Frame frequency
 t_r : Response time (rise) t_f : Response time (fall)

1.6 Backlight Characteristic

The LCD Module is backlight using a LED panel

- .Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward current	IF	TA=25°C	-	450	mA
Reverse voltage	VR	TA=25°C	-	8	V
Power dissipation	PO	TA=25°C	-	2.07	W
Operating Temperature	TOPR	-	-20	70	°C
Storage temperature	TSTG	-	-40	80	°C

- .Electrical Ratings

TA=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	VF	IF=260mA	3.8	4.2	4.6	V
Reverse current	IR	VR=8V	-	-	0.2	mA
Luminous intensity	IV	IF=260mA	22.4	28	-	cd/m ²
Wavelength	HUE	IF=260mA	571	-	576	nm
Color	Yellow Green					



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2. MODULE STRUCTURE

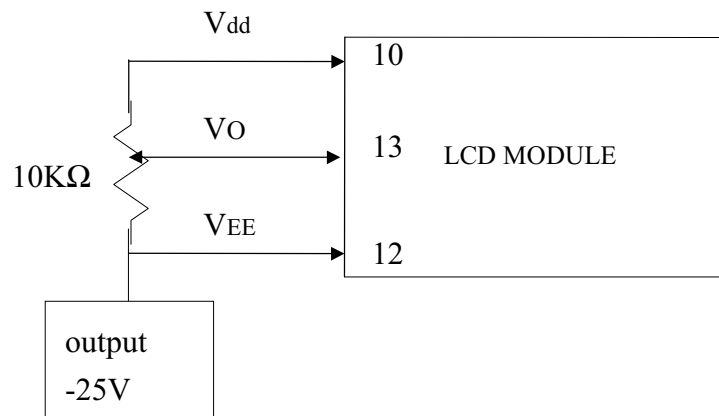
2.1 Counter Drawing

*See Appendix

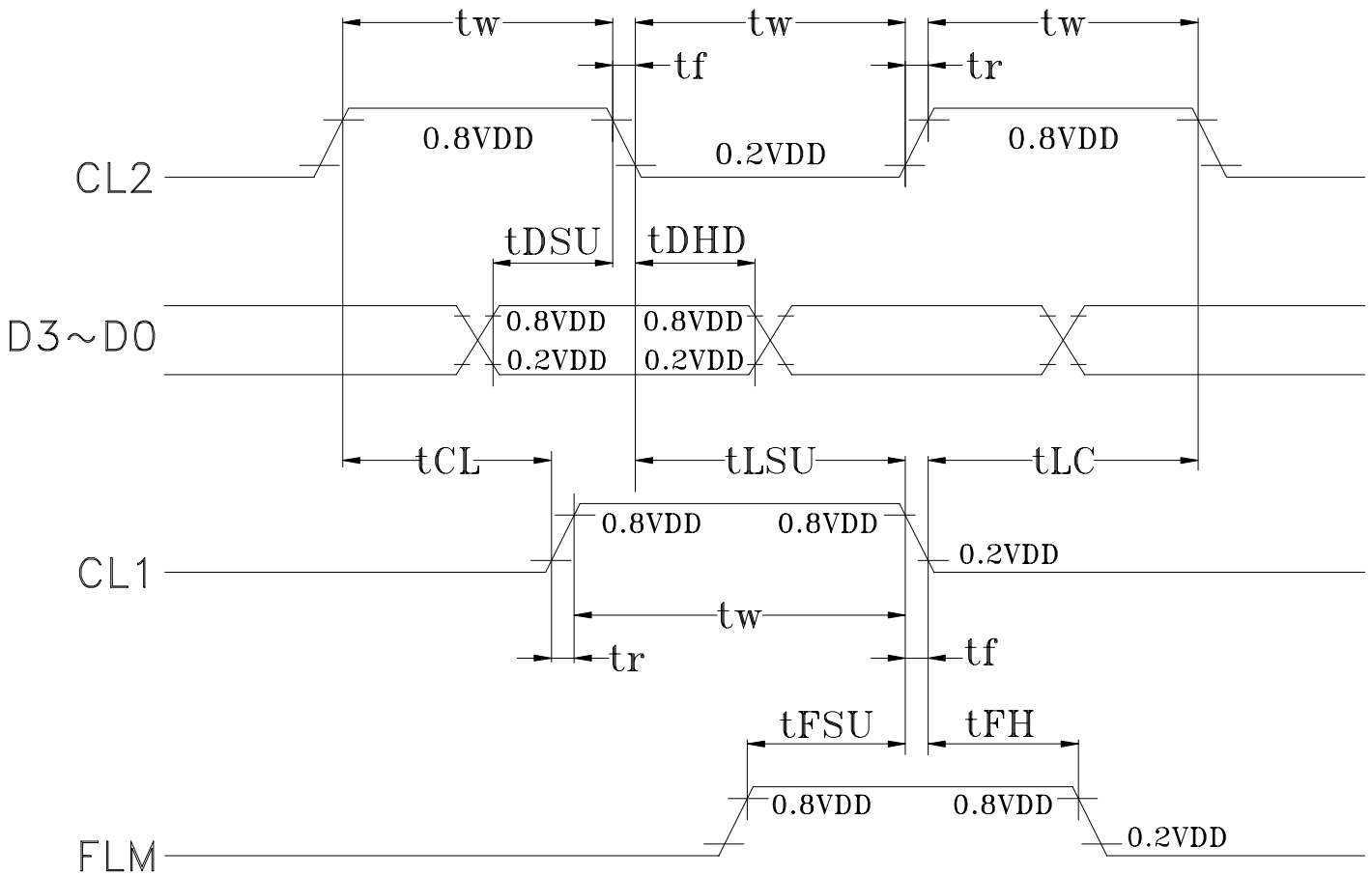
2.2 Interface Pin Description

Pin No.	Symbol	Level	Function
1	FLM	H/L	Indicates the beginning of each display cycle.
2	M	H/L	Alternation control signal
3	CL1	H,H→L	The CL1 latches the serial data in the shift registers.
4	CL2	H,H→L	Clock signal for shifting the serial data.
5	D-OFF	H/L	Display enable signal . H:ON L:OFF
6	DB0	H/L	Data bit 0 H:ON(White) L:OFF(Black)
7	DB1	H/L	Data bit 1 H:ON(White) L:OFF(Black)
8	DB2	H/L	Data bit 2 H:ON(White) L:OFF(Black)
9	DB3	H/L	Data bit 3 H:ON(White) L:OFF(Black)
10	Vdd	+5V	Power supply voltage for logic.
11	Vss	0V	Ground
12	Vee		Power supply for LC driving.
13	V0	-	Operating voltage for LC driving.
14	FG	-	Frame ground

Contrast Adjust



2.3 Timing Characteristics



Item	Symbol	Condition	Min.	Max.	Unit
Max. Clock Frequency	fCL2	Vdd=5V±5% Vss=0V Ta=25°C	8.0	-	MHZ
CL1/CL2 Pulse Width	t _w		125	-	ns
Rise/Fall Time	t _r , t _f		-	1	
Data Set-Up time	t _{DSU}		20	-	
Data Hold Time	t _{DHD}		20	-	
CL2→ CL1 Time	t _{CL}		80	-	
CL1 Set-Up Time	t _{LSU}		80	-	
CL1→ CL2 Time	t _{LC}		80	-	
FLM Set-Up Time	t _{FSU}		100	-	
FLM Hold Time	t _{FH}		100	-	



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