

***POWERTIP TECH. CORP.***  
DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification for Approval

Customer : \_\_\_\_\_

Model Type : LCD Module

Model Number : PG240128LRS-BNN-H-P1

Edi : 0

Customer Sign	Sales Sign	Approved By	Prepared By

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# 1. SPECIFICATIONS

## 1.1 Features

- Full dot-matrix structure with 240 dots \*128 dots
- 1/128 Duty, 1/12 bias
- STN LCD, positive,gray
- Transflective LCD
- 6 o'clock viewing angle
- 4 bits parallel data input ,without controller IC
- Built-in negative voltage and LED backlight

## 1.2 Mechanical Specifications

- Outline dimension : 144.0mm(L)\*104.0mm(W)\*15.0mm max.(H)
- Viewing area : 114.0mm \*64.0mm
- Active area : 107.95mm \*57.55mm
- Dot size : 0.4mm \*0.4mm
- Dot pitch : 0.45mm \*0.45mm

## 1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	VDD	-	0	7.0	V
LCD drive Supply voltage	VDD-VEE	-	-	28.0	V
Input voltage	VIN	-	-0.3	VDD+0.3	V
Operating temperature	TOPR	-	-20	70	°C
Storage temperature	TSTG	-	-30	85	°C
Humidity*1	HD	-	-	90	%RH

## 1.4 DC Electrical Characteristics

VDD=+5V±10%,VSS=0V,TA=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	VDD	-	4.5	5	5.5	V
“H” input voltage	VIH	-	0.8VDD	-	VDD	V
“L” input voltage	VIL	-	0	-	0.2VDD	V
“H” output voltage	VOH	-	VDD-0.3	-	-	V
“L” output voltage	VOL	-	-	-	0.3	V
Supply current	IOP	VDD=5V	-	-	13	mA
LCD driving voltage	VLCD	VDD-VO	-	17.5	-	V

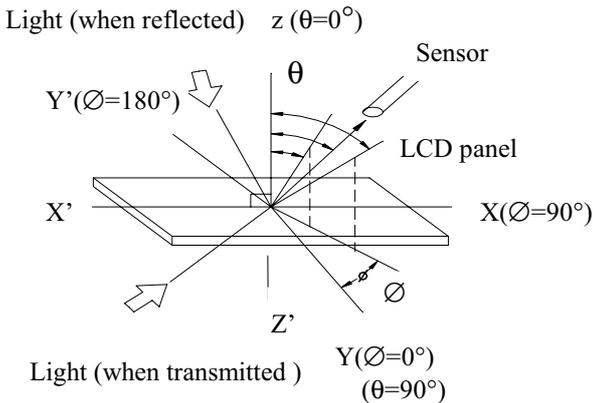


### 1.5 Optical Characteristics

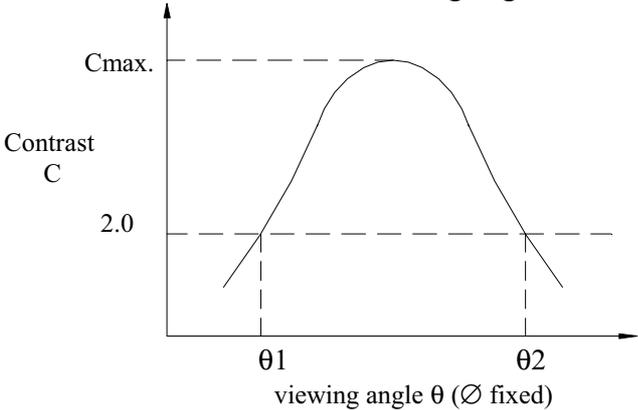
1/128 duty, 1/12 bias, Vopr=17.5V, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	$\theta$	$C \geq 2.0, \varnothing = 0^\circ C$	20°	-	-	Notes 1 & 2
Contrast	C	$\theta = 5^\circ, \varnothing = 0^\circ$	-	2.5	-	Note 3
Response time(rise)	ton	$\theta = 5^\circ, \varnothing = 0^\circ$	-	230ms	350ms	Note 4
Response time(fall)	toff	$\theta = 5^\circ, \varnothing = 0^\circ$	-	225ms	340ms	Note 4

Note 1: Definition of angles  $\theta$  and  $\varnothing$



Note 2: Definition of viewing angles  $\theta_1$  and  $\theta_2$

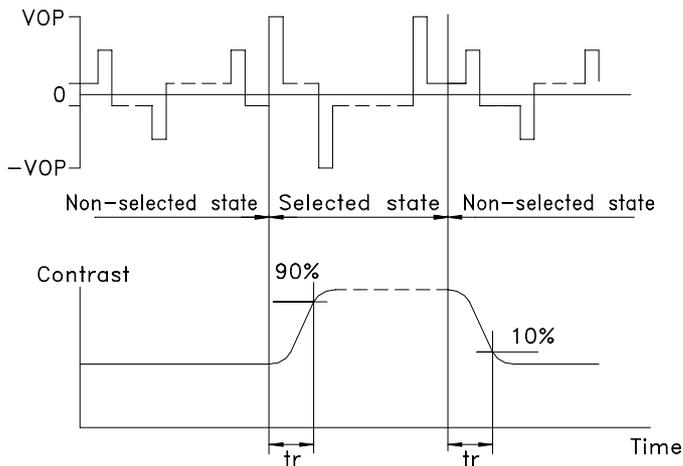
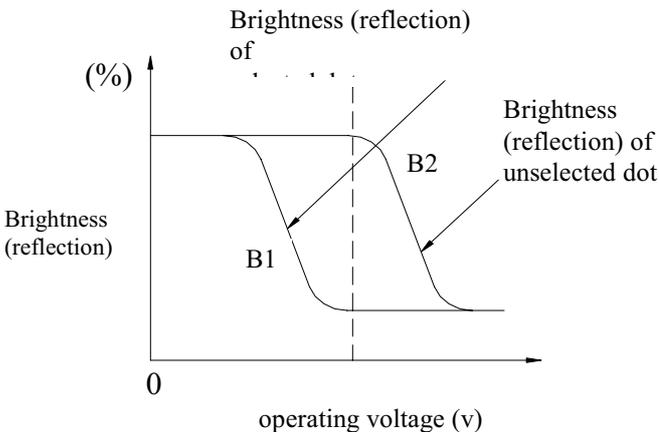


Note : Optimum viewing angle with the naked eye and viewing angle  $\theta$  at Cmax. Above are not always the

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$

Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm<sup>2</sup>

Vopr : Operating voltage      fFRM : Frame frequency  
 ton : Response time (rise)      toff : Response time (fall)

## 1.6 Backlight Characteristic

The LCD Module is backlight using a LED panel

- Maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit
Forward current	If	Ta:25°C	-	2250	mA
Reverse voltage	Vr	Ta:25°C	-	8	V
Power dissipation	Po	Ta:25°C	-	10.3	W
Operating temperature	Topr	-	-20	70	°C
Storage temperature	Tstg	-	-40	80	°C

- Electrical characteristics

Item	Symbol	Condition	Min.	Typ	Max.	Unit
Forward voltage	Vf	If:900mA	-	4.35	4.6	V
Reverse current	Ir	VR: 8V	-	-	0.2	mA
Luminous intensity	Iv	If:900mA	-	170	-	cd/m <sup>2</sup>
Wavelength	$\lambda_p$	If:900mA	-	570	-	nm
Color	Yellow Green					



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## 2. MODULE STRUCTURE

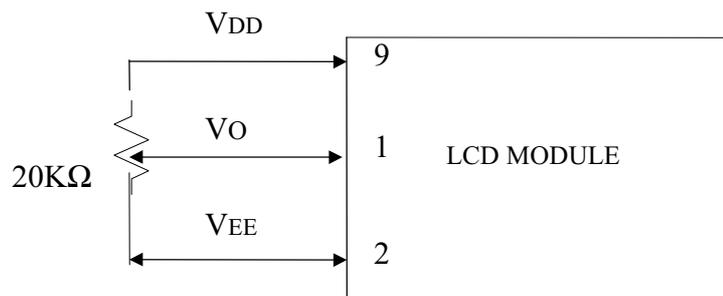
### 2.1 Counter Drawing

\*See Appendix

### 2.2 Interface Pin Description

Pin No.	Symbol	Level	Function
1	VO	-	Operating voltage for LC driving.
2	VEE	-	Power supply for LC driving.
3	D3	H/L	Data bit 3 H:ON(White) L:OFF(Black)
4	D2	H/L	Data bit 2 H:ON(White) L:OFF(Black)
5	D1	H/L	Data bit 1 H:ON(White) L:OFF(Black)
6	D0	H/L	Data bit 0 H:ON(White) L:OFF(Black)
7	M	H/L	Liquid crystal AC drive control signal
8	VSS	0V	Ground
9	VDD	+5V	Power supply voltage for logic.
10	CL2	H,H→L	Clock signal for shifting the serial data.
11	CL1	H,H→L	The CL1 latches the serial data in the shift registers.
12	FRM	H/L	Indicates the beginning for each display cycle.
13	D-OFF	H/L	Display enable signal. H:ON L:OFF
14	FG	-	Frame ground

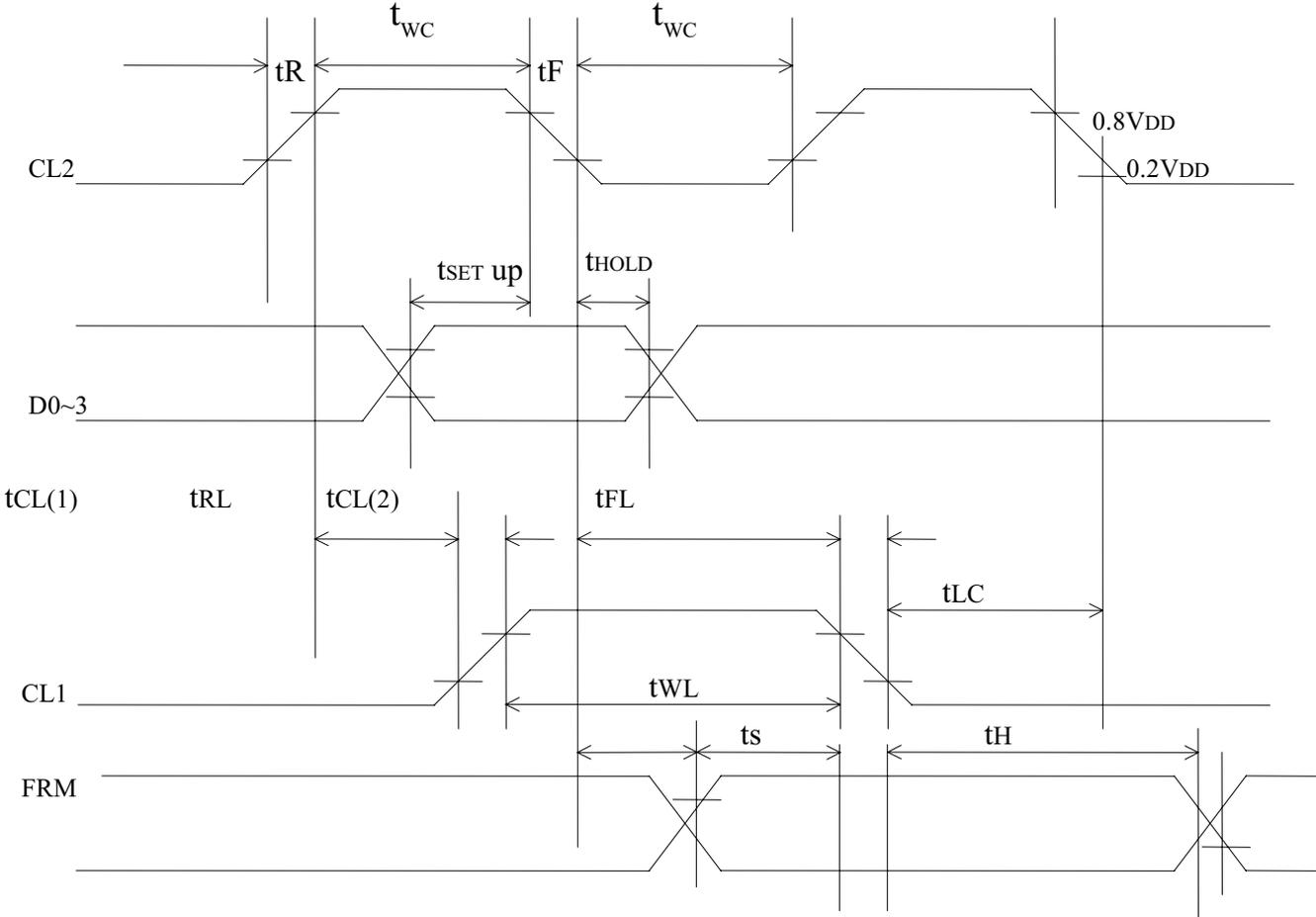
Contrast Adjust



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### 2.3 Timing Characteristics



VDD=+5V±10%,VSS=0V,TA=25°C

Item	Symbol	Condition	Min.	Max	Unit
		s			
CL2 shift clock frequency	fCP	-	-	3.3	MHZ
CL2 pulse width	tWC	-	100	-	ns
CL1 pulse width	tWL	-	100	-	ns
D0~D3 to CL2 setup time	tSETUP	-	80	-	ns
D0~D3 to CL2 hold time	tHOLD	-	80	-	ns
CL2 to CL1 time	tCL1	-	0	-	ns
	tCL2	-	100	-	
CL1 to CL2 time	tLC	-	100	-	ns
CL2 rise time	tR	-	-	50	ns
CL2 fall time	tF	-	-	50	ns
CL1 rise time	tRL	-	-	50	ns
CL1 fall time	tFL	-	-	50	ns
FRM setup time	tS	-	100	-	ns
FRM Hold time	tH	-	100	-	ns



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