

POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

【產品規格書】

Customer : _____

Model Type : LCD Module

Sample Code : PG192128LRS-BYA-B-S0

Mass Production Code : _____

Edition : 0

Customer Sign	Sales Sign	Approved By	Prepared By

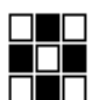
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1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 192 dots *128 dots
- 1/128 Duty, 1/12 bias
- STN LCD, positive, gray display
- Transflective LCD
- 6 o'clock viewing angle
- Controller IC LC7981 , 8 bits parallel data input
- Built-in negative voltage generator circuit
- With LED backlight

1.2 Mechanical Specifications

- Outline dimension : 98.0mm(L)*86.0mm(W)*13.4mm (H) max
- Viewing area : 77.5mm*54.0mm
- Active area : 71.0mm*47.32mm
- Dot size : 0.33mm*0.33mm
- Dot pitch : 0.37mm*0.37mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	VDD	-	0	7.0	V
LCD drive Supply voltage	VDD- VEE	-	-	28	V
Input voltage	VIN	-	-0.3	VDD+0.3	V
Operating temperature	TOPR	-	0	50	°C
Storage temperature	TSTG	-	-10	60	°C
Humidity	HD	-	-	90	%RH

1.4 DC Electrical Characteristics

VDD=+5V±10%, VSS=0V, TA=25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	VDD	-	4.5	5	5.5	V
“H” input voltage	VIH	-	0.8VDD	-	VDD	V
“L” input voltage	VIL	-	0	-	0.2VDD	V
“H” output voltage	VOH	-	VDD-0.4	-	-	V
“L” output voltage	VOLI	-	-	-	0.4	V
Supply current	IDD	VDD=5V	-	36.0	42.0	mA
LCD driving voltage	VOP	VDD- VO	-	18.36	19.64	V



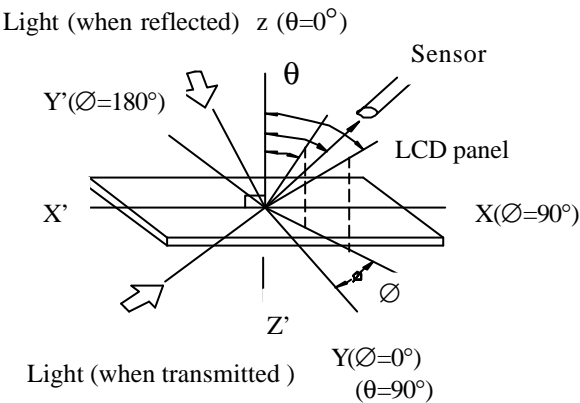
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1.5 Optical Characteristics

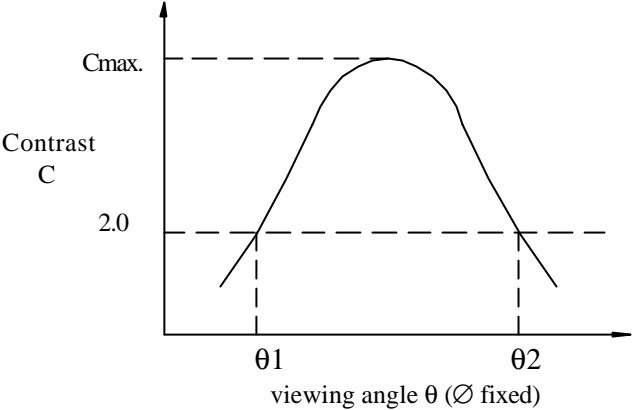
1/128 duty, 1/12 bias, $V_{OPR}=19.1V$, $T_a=25^{\circ}C$

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	$C \geq 2.0, \varnothing = 0^{\circ}$	30°	-	-	Notes 1 & 2
Contrast	C	$\theta = 5^{\circ}, \varnothing = 0^{\circ}$	-	3	-	Note 3
Response time(rise)	T_r	$\theta = 5^{\circ}, \varnothing = 0^{\circ}$	-	200ms	300ms	Note 4
Response time(fall)	T_f	$\theta = 5^{\circ}, \varnothing = 0^{\circ}$	-	250ms	400ms	Note 4

Note 1: Definition of angles θ and \varnothing



Note 2: Definition of viewing angles θ_1 and θ_2

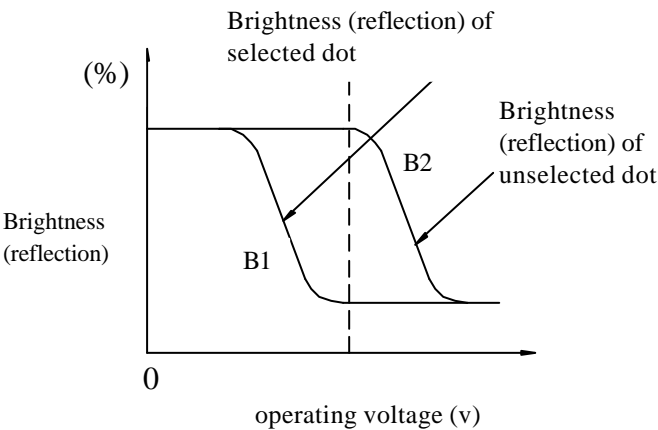


Note : Optimum viewing angle with the naked eye and viewing angle θ at C_{max} . Above are not always the same

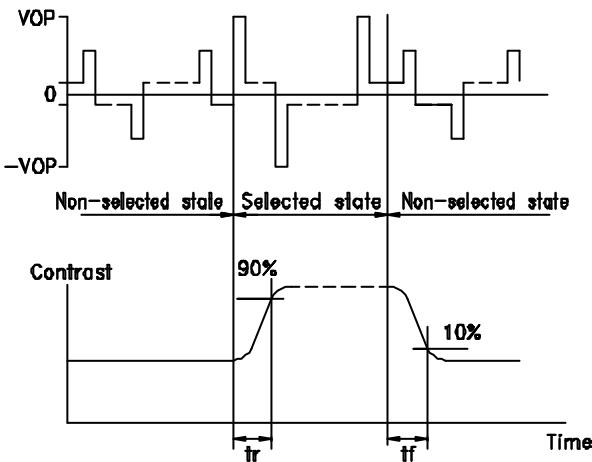
Note 3: Definition of contrast C

Brightness (reflection) of unselected dot (B2)

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note: Measured with a transmissive LCD panel which is displayed 1 cm²

V_{OPR} : Operating voltage
 t_r : Response time (rise)

f_{FRM} : Frame frequency
 t_f : Response time (fall)



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1.6 Backlight Characteristic

The LCD Module is backlight using a LED panel

•.Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward current	IF	TA=25°C	-	350	mA
Reverse voltage	VR	TA=25°C	-	8	V
Power dissipation	PO	TA=25°C	-	1.54	W
Operating Temperature	TOPR	-	-20	70	°C
Storage temperature	TSTG	-	-40	80	°C

•.Electrical Ratings

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	VF	IF=140mA	-	4.0	4.4	V
Reverse current	IR	VR=8V	-	-	0.2	mA
Luminous intensity (without LCD)	IV	IF=140mA	14.4	18	-	cd/m ²
Luminous intensity (with LCD)	IV	IF=140mA	-	2.94	-	cd/m ²
Wavelength	HUE	IF=140mA	571	-	576	nm
Color	Yellow Green					



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2. MODULE STRUCTURE

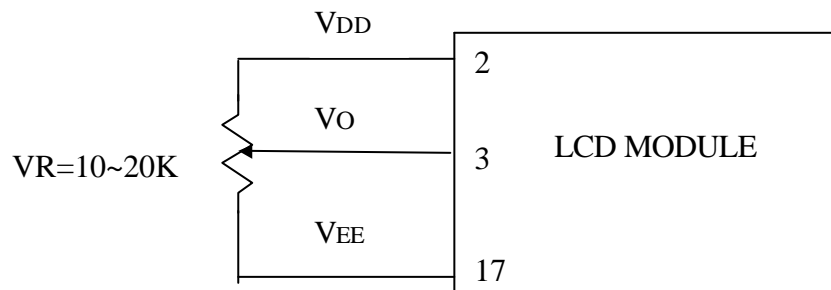
2.1 Counter Drawing

*See Appendix 1

2.2 Interface Pin Description

Pin No.	Symbol	Signal Description
1	VSS	Power Supply ($V_{SS}=0$)
2	VDD	Power Supply ($V_{DD}>V_{SS}$)
3	Vo	Operating voltage for LCD
4	RS	Register Select-High =Instruction, Low =Data
5	$\overline{R/W}$	Read/Write Low =MPU to LCM, High =LCM to MPU
6	E	Enable $\overline{R/W}$ =Low: Data is written on the falling edge of E $\overline{R/W}$ =High: Data can be read at E=1
7~14	DB0 to DB7	Data bus
15	\overline{CS}	Chip select
16	\overline{RES}	Reset signal
17	VEE	Negative voltage output
18	NC	NC
19	A	Power supply LED backlight (+)
20	K	Power supply LED backlight (-)

Contrast Adjust



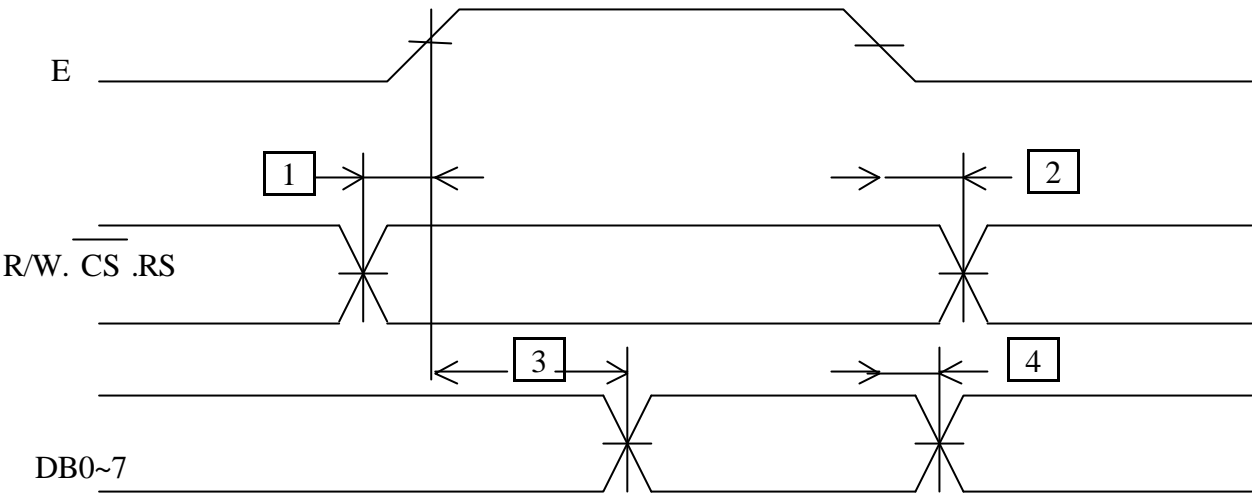
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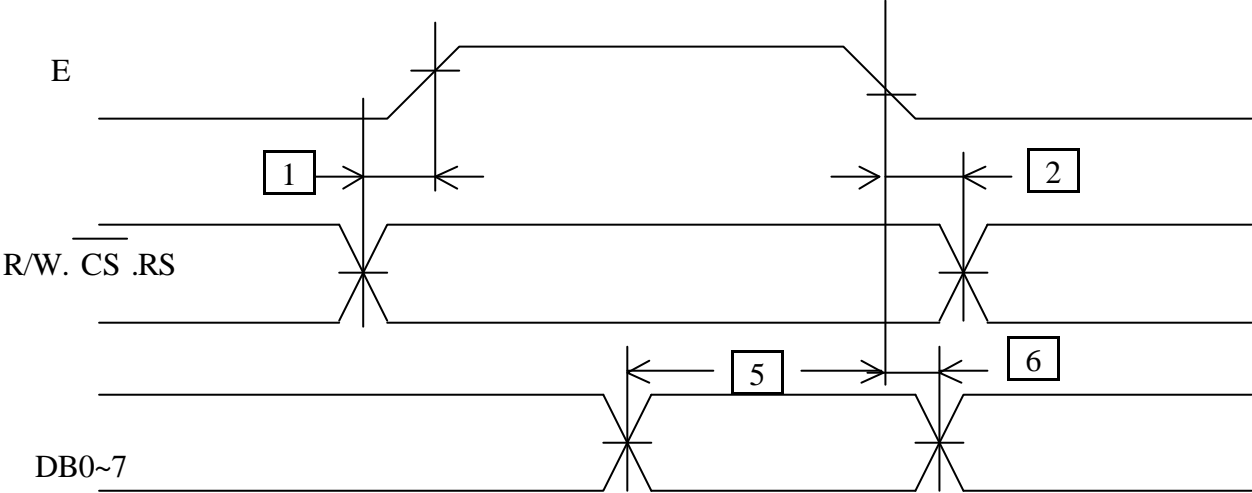
2.3 Timing Characteristics

- Bus read/write timing

Read cycle



Write cycle



TA=-20 to +75°C, VDD= 5V±5%, GND= 0V

No	Item	Symbol	Min.	typ	Max.	Unit	Conditions
1	Address set-up time	tAS	90	-	-	ns	-
2	Address hold time	tAH	10	-	-	ns	-
3	Data delay time(read)	tDDR	-	-	140	ns	CL=50pF
4	Data hold time (read)	tDHR	10	-	-	ns	-
5	Data set-up time (write)	tDSW	220	-	-	ns	-
6	Data hold time (write)	tDHW	20	-	-	ns	-



2.4 Display command

- Display control instruction

Display is controlled by writing data into the instruction register and 13 data registers. The instruction register and the data register are distinguished by the RS signal. First, write 4-bit data

in the instruction register when RS=1, then specify the code of the data register. Next with RS=0, write 8-bit data in the data register, which executes the specify instruction.

A new instruction cannot be accepted while an old instruction is being executed. As the Busy flag is set under this condition, write an instruction only after reading the Busy flag and making sure that it is 0.

However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction. The Busy flag does not change when data is written into the instruction register (RS=1). Therefore, the Busy flag need not be checked immediately after writing data into the instruction register.

(1) Mode control

Write code "00H" (in hexadecimal notation) in the instruction register and specify the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	0	0
Mode control Reg	0	0	0	0	MODE Data					

DB5	DB4	DB3	DB2	DB1	DB0	Cursor / blink	CG	Graphic/character display
1 / 0	1 / 0	0	0	0	0	Cursor OFF	Built-in CG	Character display
		0	1			Cursor ON		
		1	0			Cursor OFF		
		1	1			Cursor blink		
		0	0		1	Cursor OFF	External CG	
		0	1			Cursor ON		
		1	0			Cursor OFF character blink		
		1	1			Cursor blink		
		0	0	1	0			Graphic mode
		Display ON/OFF	Master/slave	Blink	Cursor	Mode	External/ builtin CG	

1: master mode

0: slave mode

1: display ON

0: display OFF



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(2) Setting the character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	0	1
Character pitch Reg	0	0	(Vp-1) Binary				0	(Hp-1) Binary		

Vp is the number of vertical dots per character. Determine Vp with the pitch between two vertically placed characters taken into consideration. This value is meaningful only in the character display mode: It is invalid in the graphic mode.

In character mode, Hp indicates the number of horizontal dots per character, from the leftmost part of one character to the leftmost part of the next. In the graphic mode, Hp indicates how many bits (or dots) from RAM appear in a 1-byte display.

Hp must take one of the following three values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	Horizontal character pitch 7
8	1	1	1	Horizontal character pitch 8

(3)Setting the number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	1	0
Character number Reg	0	0	(HN - 1) Binary (239)							

In the character display mode, HN indicates the number of characters in the horizontal direction. In the graphic mode, it indicates the number of bytes in the horizontal direction. The total number of dots positioned horizontally on the screen n is given by the formula

$$n = H_p * H_N.$$

Even numbers in the range 2 to 256 (decimal) can be set as HN.

(4) Setting the time division number (display duty)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	1	1
Time division Reg	0	0	(Nx - 1) Binary (127)							

Consequently, $1/N_x$ is the display duty.

Decimal numbers within the range 1 to 256 can be set as Nx.

(5)Setting the cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	1	0	0
Cursor position Reg	0	0	0	0	0	0	(Cp - 1) Binary			



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In the character display mode, Cp indicates the line at which the cursor is displayed. For example, when Cp=8 (decimal) is specified, the cursor is displayed beneath the character of the 5*7 dot-font. The horizontal length of the cursor equals Hp (the horizontal character pitch). Decimal values in the range 1 to 16 can be assigned to Cp. When the value is less than the vertical character pitch Vp ($Cp \leq Vp$), display priority is given to the cursor (provided the cursor display is ON). The cursor is not displayed when $Cp > Vp$. The horizontal length of the cursor equals Hp.

(6)Setting the display start lower address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	0	0
Mode control Reg	0	0	(start address lower byte) binary							

(7)Setting the display start upper address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	0	1
Display start address Reg (lower byte)	0	0	(start address upper byte) binary							

This instruction writes the display start address value in the display start address register. The display start address at which data to be displayed at the leftmost position of the top line of the screen is stored. The start address consists of 16 bit (upper and lower).

(8)Setting the cursor (lower) address (RAM read/write lower address)

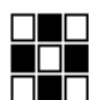
Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	1	0
Cursor address counter (lower byte)	0	0	(cursor address lower byte) binary							

(9)Setting the cursor (upper) address (RAM read/write lower address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	1	1
Cursor address counter (upper byte)	0	0	(cursor address upper byte) binary							

This instruction writes the cursor address value in the cursor address counter. The cursor address indicates the address for exchanging display data and character codes with RAM. In other words, data at the address specified by the cursor address is read from or written into RAM. In character display, the cursor is displayed at the position specified by the cursor address.

The cursor address is divided into a lower address (8 bits) and an upper address (8 bits). It should



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be set in accordance with the following rules.

1	To rewrite (set) both lower and upper addresses:	First set the lower address, then the upper.
2	To rewrite the lower address:	Always reset the upper address after setting the lower address.
3	To rewrite the upper address only:	Set the upper address. It is necessary to reset the lower address.

The cursor address counter is a 16-bit up-counter with set/reset functions: when the Nth bit goes from 1 to 0, the count of the (N + 1)th bit increments by one. Accordingly, when the lower address is set so that the lower MSB (8th bit) changes from 1 to 0, the LSB (1st bit) of the upper counter must increment by one. When setting the cursor address, set the lower and upper addresses as a 2-byte continuous instruction.

(10)Writing display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code)							LSB

Write code “0DH” in the instruction register. Then, Write 8-bit data with RS=0, and the data is written into RAM as display data or character codes at the address specified by the cursor address counter. After writing, the count of the cursor address counter increments by 1.

(11)Reading display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code)							LSB

Write “0CH” in the instruction register. Then, establish the read status with RS=0, and data in the RAM can be read. The procedure for reading data is as follows:

This instruction outputs the contents of the data output register to DB0 to 7, then transfers the RAM data indicated by the cursor address to the data output register. It then increments the cursor address by 1, which means that correct data cannot be read in the first read operation. The specified value is output in the second read operation. Accordingly, a dummy read operation must be performed once when reading data after setting the cursor address.

(12)Bit clear

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	1	0
Bit clear	0	0	0	0	0	0	0	(NB - 1) Binary		



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(13)Bit set

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	1	1
Bit set	0	0	0	0	0	0	0	(NB - 1) Binary		

As the bit-clear or bit-set instruction, 1 bit of a 1 byte of data in display RAM is set to 0 or 1. The bit specified by NB is set to 0 for the bit-clear instruction and 1 for the bit-set instruction. The RAM address is specified by the cursor address, which is automatically incremented by 1 at the completion of the instruction. NB is a value in the range from 1 to 8. The LSB is indicated by NB=1, and the MSB by NB=8.

(14)Reading the BUSY flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
busy flag	1	1	1/0	*						

The Busy flag is output to DB7 when read mode is established with RS=1. The Busy flag is set to 1 while any of the instructions (1) through (13) is being executed. It is set to 0 at the completion of the execution, allowing the next instruction to be accepted. No other instruction can be accepted when the Busy flag is 1.

Accordingly, before writing an instruction and data, it is necessary to ensure that the Busy flag is 0. However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction.

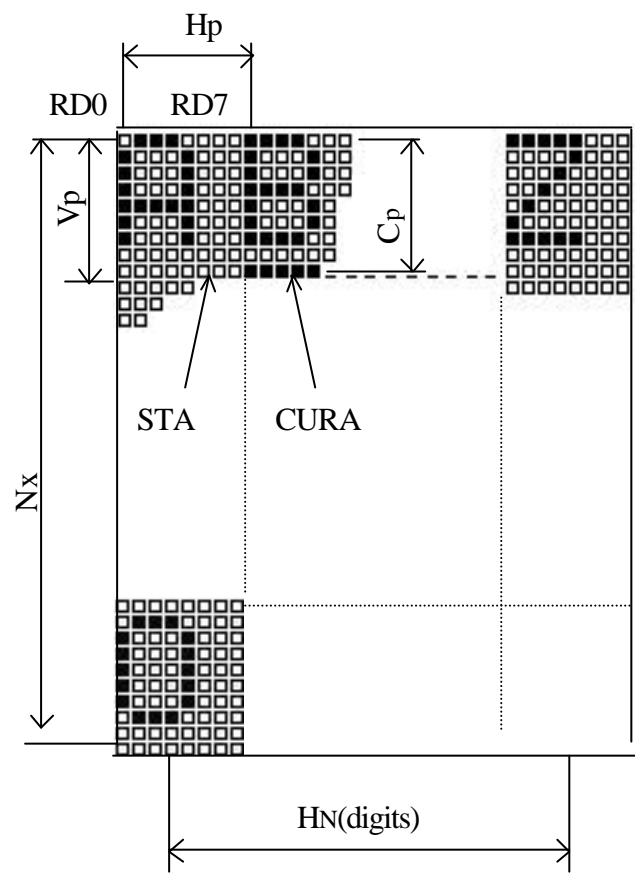
The Busy flag does not change when data is written into the instruction register (RS=1). Therefore, the Busy Specification of the instruction register is unnecessary to read the Busy flag.



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The relation between the LCD panel display and Hp, HN, Vp, Cp, Nx



Symbol	Description	Contents	Value
Hp	Horizontal character' pitch	Character pitch in the horizontal direction	6 to 8 dots
HN	Number of characters in the horizontal direction	Number of characters (digits) per horizontal line or the number of words per line (graphic)	Even digits in the range 2 to 256
Vp	Vertical character pitch	Character pitch in the vertical direction	1 to 16 dots
Cp	Cursor position	The line number at which the cursor is to be display	1 to 16 line
Nx	Number of lines in the vertical direction	Display duty	1 to 256 lines

(Note)
When the number of vertical dots on the screen is m and that of horizontal dots is n,
 $1/m=1/Nx$ =display duty
 $n=Hp*HN$
 m/Vp =number of display lines
 $Cp\leq Vp$



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Display mode

Display Mode	Display data from the MPU	RAM	LC panel																								
Character display	Display pattern (8 bits)	<div><p>b7 b6 b5 b4 b3 b2 b1 b0</p><table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table><p>Start address</p></div>									0	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	<div><p>Hp</p><p>A B C</p><p>Hp: 6, 7 or 8 dots</p></div>
0	1	0	0	0	0	0	1																				
0	1	0	0	0	0	1	0																				
Graphic	Character code (8 bits)	<div><p>Hp</p><p>b7 b6 b5 b4 b3 b2 b1 b0</p><table><tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table><p>Start address</p></div>									0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	<div><p>b0 b7 Hp</p><p>8 dots 8 dots</p><p>Hp: 8 dots</p></div>
0	1	0	1	0	1	0	1																				
1	1	1	1	1	1	1	1																				



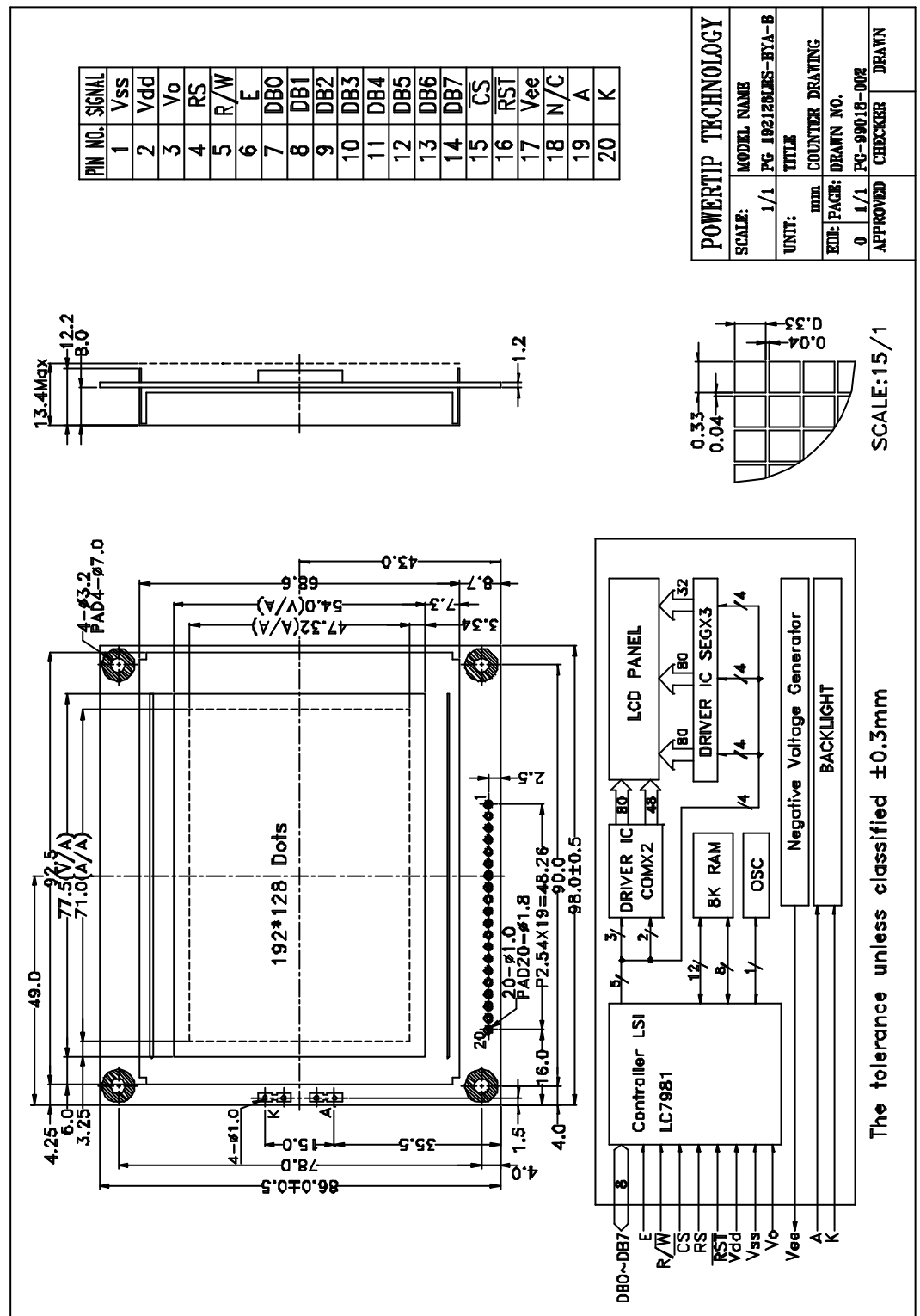
2.5 Character Pattern

Upper 4bit Lower 4bit	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
xxxx0000		0	a	P	`	P		-	9	E	a	p
xxxx0001	!	1	A	Q	a	9	.	7	+	4	a	q
xxxx0010	"	2	B	R	b	r	'	4	9	x	p	θ
xxxx0011	#	3	C	S	c	s]	9	7	e	e	∞
xxxx0100	\$	4	D	T	d	t	\	I	+	+	μ	o
xxxx0101	%	5	E	U	e	u	.	7	+	1	e	0
xxxx0110	&	6	F	V	f	v	9	9	+	+	p	Σ
xxxx0111	'	7	G	W	g	w	7	+	+	7	g	π
xxxx1000	(8	H	X	h	x	4	9	+	+	5	x
xxxx1001)	9	I	Y	i	y	+	7	+	+	'	y
xxxx1010	*	:	J	Z	j	z	±	+	+	+	j	*
xxxx1011	+	:	K	C	k	(+	9	+	+	+	π
xxxx1100	,	<	L	*	1	1	+	9	+	+	+	π
xxxx1101	-	=	M	I	m)	+	+	+	+	+	÷
xxxx1110	.	>	N	^	n	+	+	+	+	+	+	+
xxxx1111	/	?	O	L	o	+	+	+	+	+	+	+



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