International
IOR Rectifier

January 28, 2009

Automotive Grade AUIRS2003S

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
- Fully operational to +200V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10V to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- High-side output in phase with HIN input
- Low-side output out of phase with $\overline{\text{LIN}}$ input
- Leadfree, RoHS compliant
- Automotive qualified*

Typical Applications

- Pre-charge Switch Drives
- Stepper / Motor Drives
- DC-DC Converters

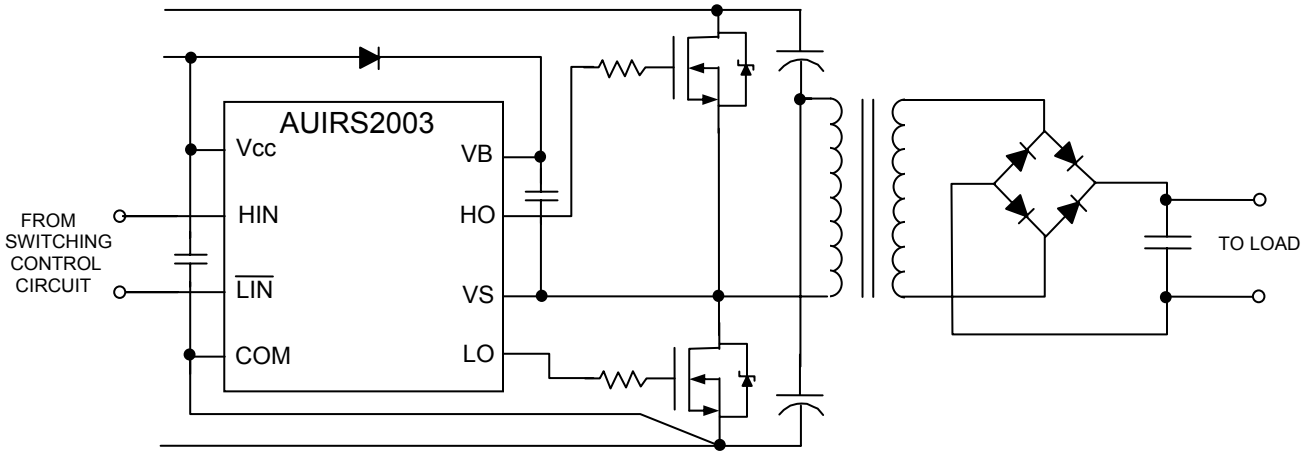
Product Summary

Topology	General Driver
V_{OFFSET}	≤ 200V
V_{OUT}	10V – 20V
I_{o+} & I_{o-} (typical)	290mA & 600mA
t_{on} & t_{off} (typical)	680ns & 150ns
Deadtime (typical)	520ns

Package Options

8 - Lead SOIC
AUIRS2003S

Diagram for DC-DC converter application

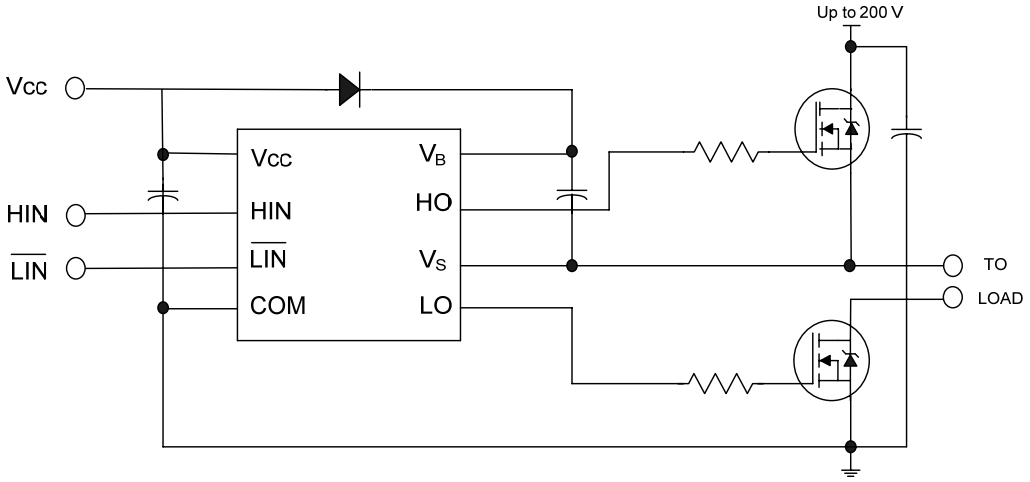


* Qualification standards can be found on IR's web site www.irf.com

Description

The AUIRS2003S is a high voltage, high speed power MOSFET and IGBT driver with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 200V.

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8N	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (per AEC-Q100-003)	
	Human Body Model	Class H2 (per AEC-Q100-002)	
	Charged Device Model	Class C5 (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level B (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/
†† Exceptions to AEC-Q100 requirements are noted in the qualification report.
††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating absolute voltage	-0.3	225	V
V_S	High side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	—	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient	—	200	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	†	200	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

† Logic operational for V_S of -5V to +200V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DR97-3 for more details).

Dynamic Electrical Characteristics

V_{CC} = V_{BS} = 15V, C_L = 1000pF, T_A = 25°C unless otherwise specified.

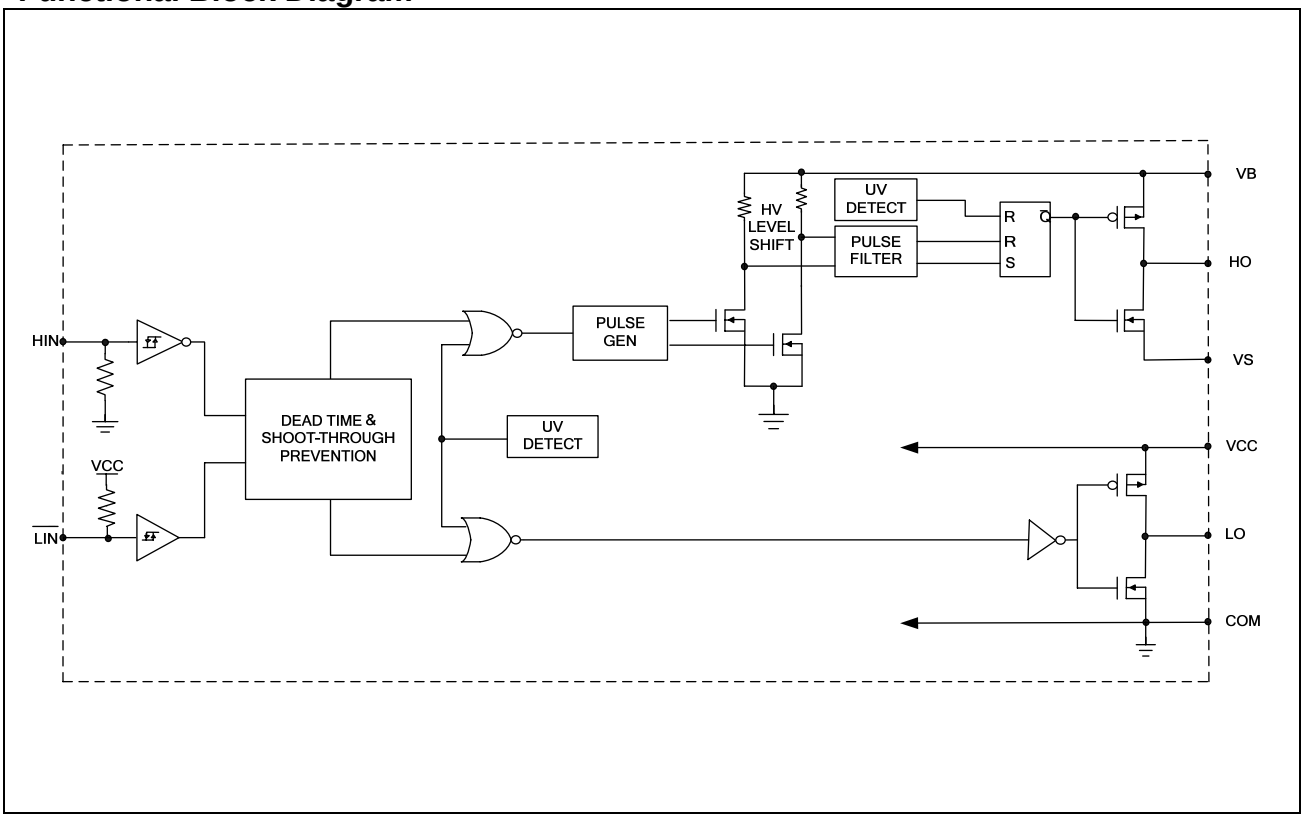
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	820	ns	V_S = 0V
t_{off}	Turn-off propagation delay	—	150	220		V_S = 200V
t_r	Turn-on rise time	—	70	170		
t_f	Turn-off fall time	—	35	90		
DT	Deadtime, LO turn-off to HO turn-on & HO turn-on to LO turn-off	400	520	650		
MT	Delay matching , HO & LO turn-on/off	—	—	60		

Static Electrical Characteristics

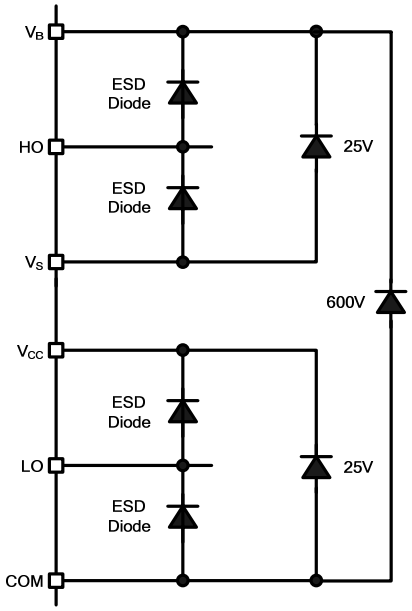
V_{CC} = V_{BS} = 15V and T_A = 25°C unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicaple to the input leads: HIN and $\overline{\text{LIN}}$. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

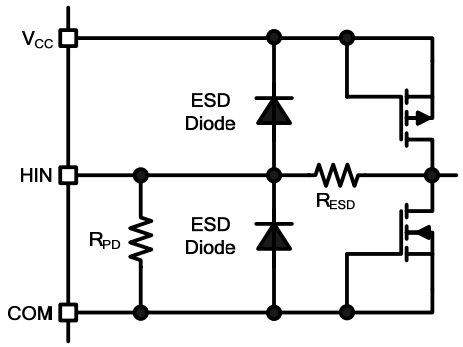
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic “1” input voltage	2.5	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage	—	—	0.8		
V_{OH}	High level output voltage, V_{CC} or V_{BS} - V_O	—	0.05	0.2		I_O = 2mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 200V
I_{QBS}	Quiescent V_{BS} supply current	—	30	55		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	—	150	270		
I_{IN+}	Logic “1” input bias current	—	3	10		V_{IN} = 5V
I_{IN-}	Logic “0” input bias current	—	—	5		V_{IN} = 0V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
I_{O+}	Output high short circuit pulsed current	130	290	—	mA	V_O = 0V, V_{IN} = V_{IH} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	270	600	—		V_O = 15V, V_{IN} = V_{IL} PW ≤ 10 µs

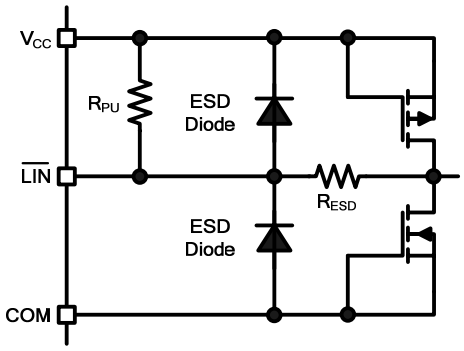
Functional Block Diagram



Input/Output Pin Equivalent Circuit Diagrams



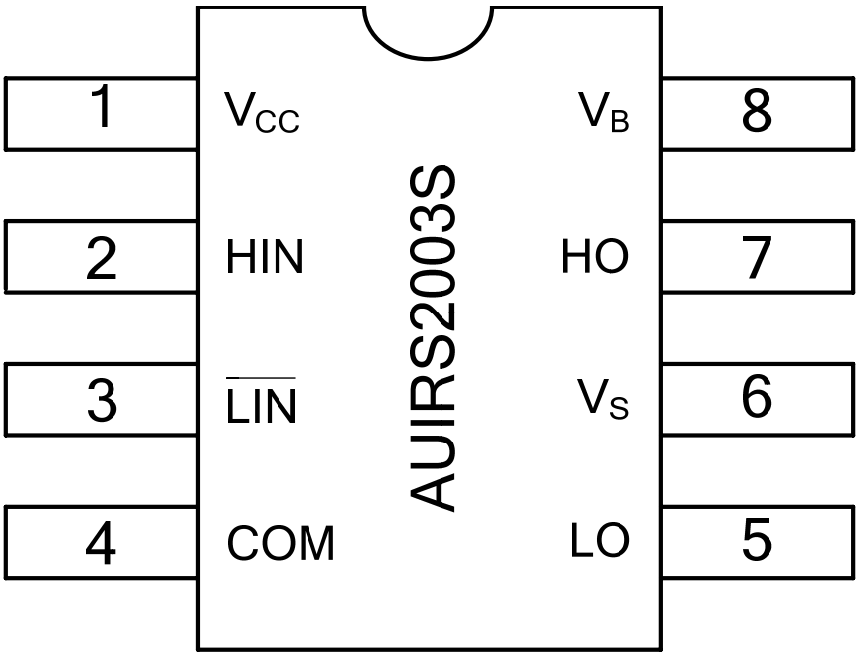




Lead Definitions

PIN	Symbol	Description
1	V_{CC}	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	$\overline{LIN}$	Logic input for low side driver output (LO), out of phase
4	COM	Low side return
5	LO	Low side gate drive output
6	V_S	High side floating supply return
7	HO	High side gate drive output
8	V_B	High side floating supply

Lead Assignments



Application Information and Additional Details

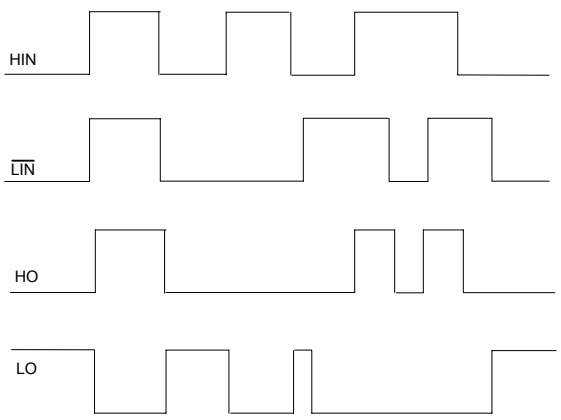


Figure 1: Input/Output Timing Diagram

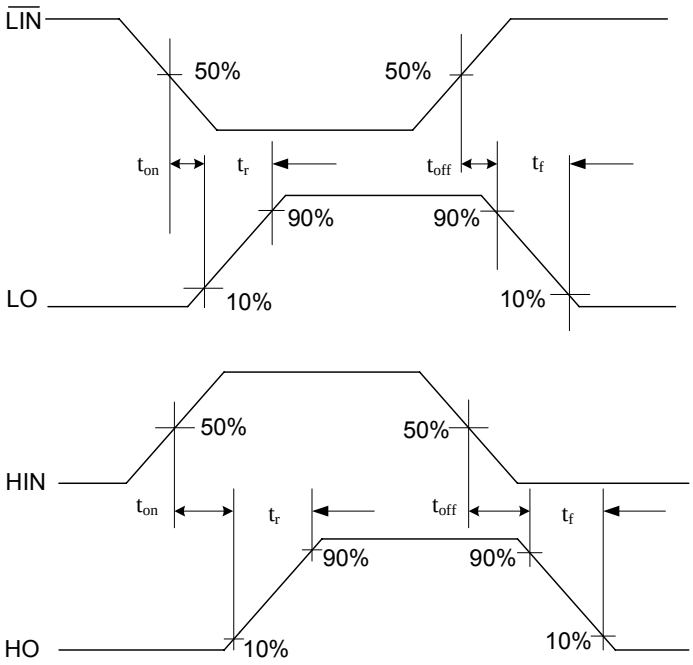


Figure 2: Switching Time Waveform Definition

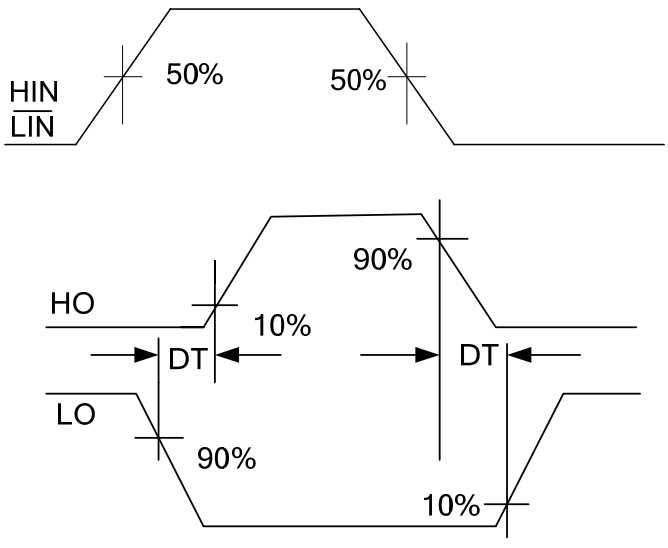
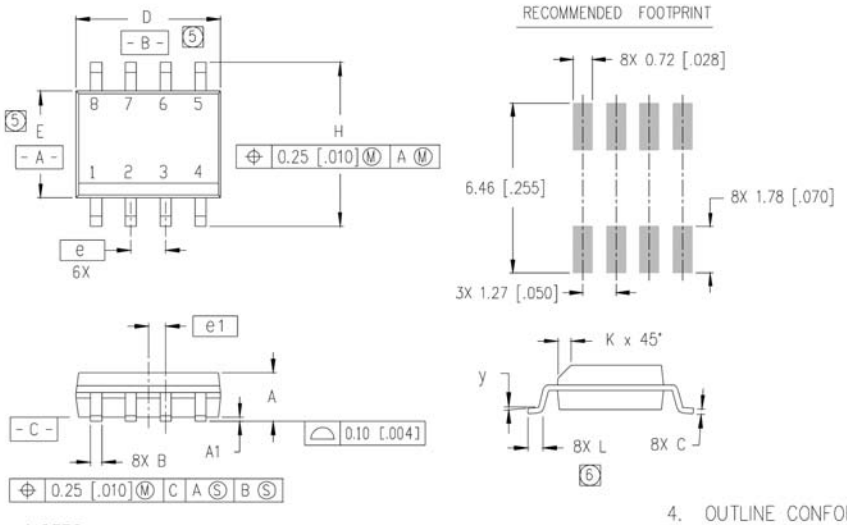


Figure 3: Delay Matching Waveform Definitions

Package Details: SOIC8N



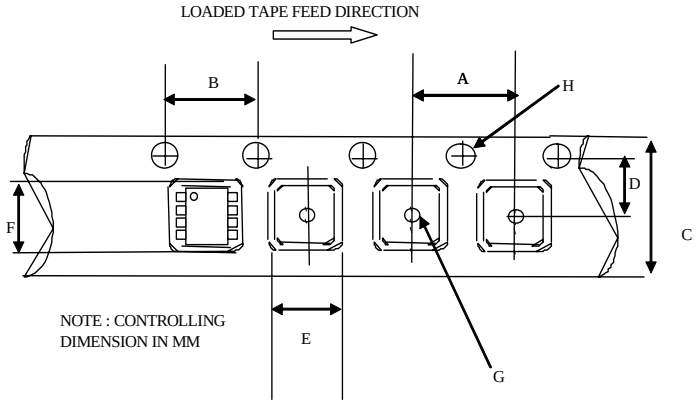
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

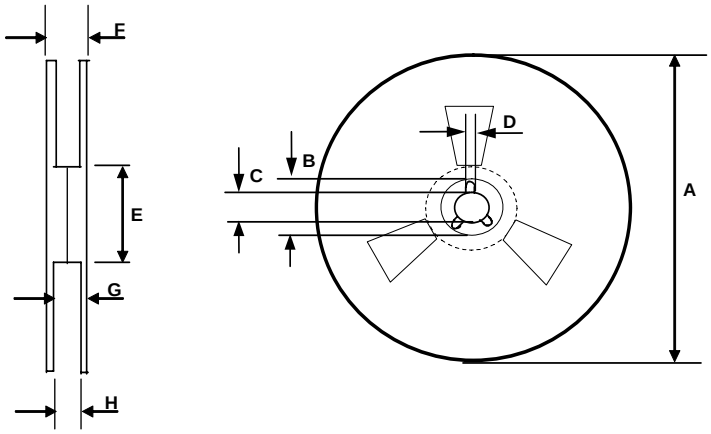
8 Lead SOIC

Package Details: SOIC8N, Tape and Reel



CARRIER TAPE DIMENSION FOR 8SOICN

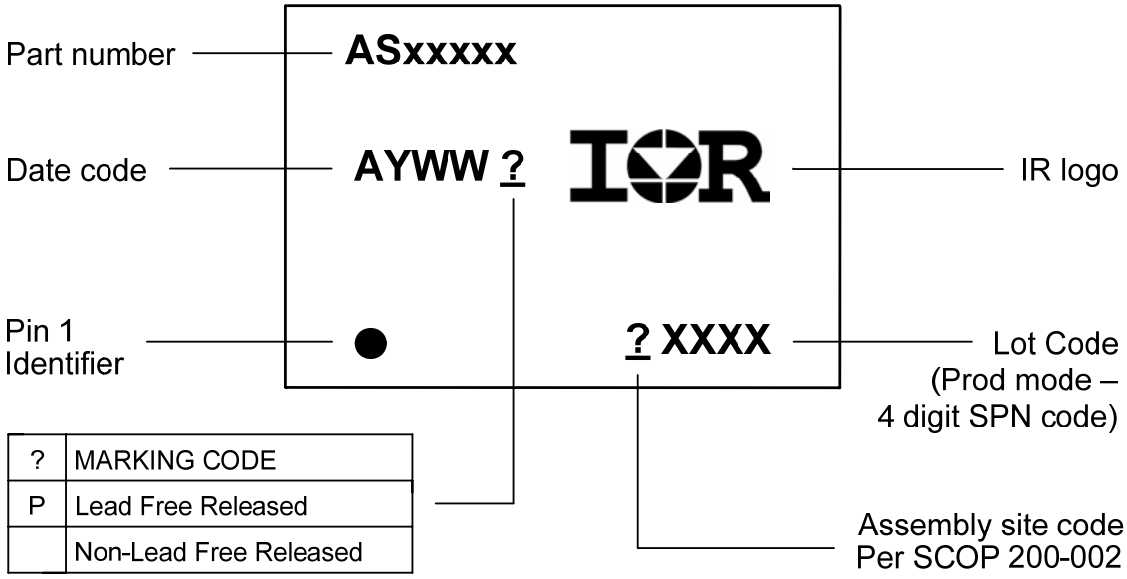
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2003S	SOIC8	Tube/Bulk	95	AUIRS2003S
		Tape and Reel	2500	AUIRS2003STR

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

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