Dual Channel Line Receiver Hermetically Sealed Optocoupler

Data Sheet

HCPL-1930, HCPL-1931, HCPL-193K, 5962-89572

Description

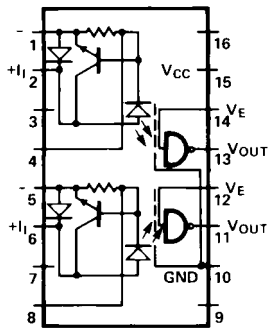
The HCPL-193X devices are dual channel, hermetically sealed, high CMR, line receiver optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a standard product or with full MIL-PRF-38534 Class Level H or K testing, or from the DSCC Standard Microcircuit Drawing (SMD) 5962-89572. This sixteen pin DIP may be purchased with a variety of lead bend and plating options. See selection guide table for details. Standard Microcircuit Drawing (SMD) parts are available for each lead style.

Truth Table

(POSITIVE LOGIC)

INPUT	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H

Functional Diagram



Features

- Dual marked with device part number and DSCC standard microcircuit drawing
- Manufactured and tested on a MIL-PRF-38534 certified line
- QML-38534, Class H and Class K
- Hermetically sealed 16-pin dual in-line package
- Performance guaranteed over full military temperature range: -55°C to +125°C
- High speed – 10 Mb/s
- Accepts a broad range of drive conditions
- Adaptive line termination included
- Internal shield provides excellent common mode rejection
- External base lead allows "LED Peaking" and LED current adjustment
- 1500 Vdc withstand test voltage
- High radiation immunity
- HCPL-2602 function compatibility
- Reliability data available

Applications

- Military and space
- High reliability systems
- Isolated line receiver
- Simplex/multiplex data transmission
- Computer-peripheral interface
- Microprocessor system interface
- Harsh environmental environments
- Digital isolation for A/D, D/A conversion
- Current sensing
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement

The connection of a 0.1 µF bypass capacitor between pins 15 and 10 is recommended.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DSCC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each unit contains two independent channels, consisting of a GaAsP light emitting diode, an input current regulator, and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance. The regulator allows a typical LED current of 12.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of +1000 V/µsec.

DC specifications are compatible with TTL logic and are guaranteed from -55°C to +125°C allowing trouble-free interfacing with digital logic circuits. An input current of 10 mA will sink a six gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

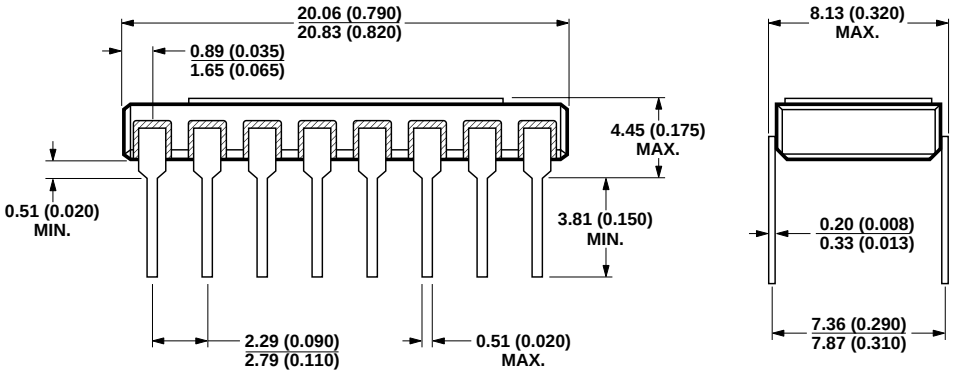
Selection Guide—Lead Configuration Options

Avago Part # and Options	
Commercial	HCPL-1930
MIL-PRF-38534 Class H	HCPL-1931
MIL-PRF-38534 Class K	HCPL-193K
Standard Lead Finish	Gold
Solder Dipped*	Option #200
Butt Joint/Gold Plate	Option #100
Gull Wing/Soldered*	Option #300
Crew Cut/Gold Plate	Option #600
Class H SMD Part #	
Prescript for all below	5962-
Either Gold or Soldered	8957201EX
Gold Plate	8957201EC
Solder Dipped*	8957201EA
Butt Joint/Gold Plate	8957201YC
Butt Joint/Soldered*	8957201YA
Gull Wing/Soldered*	8957201XA
Crew Cut/Gold Plate	Available
Crew Cut/Soldered*	Available
Class K SMD Part #	
Prescript for all below	5962-
Either Gold or Soldered	8957202KEX
Gold Plate	8957202KEC
Solder Dipped*	8957202KEA
Butt Joint/Gold Plate	8957202KYC
Butt Joint/Soldered*	8957202KYA
Gull Wing/Soldered*	8957202KXA

*Solder contains lead.

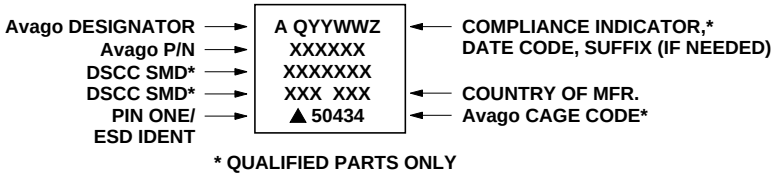
Outline Drawings

16 Pin DIP Through Hole, 2 Channels



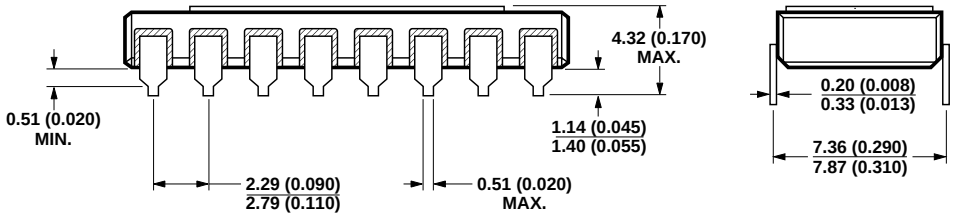
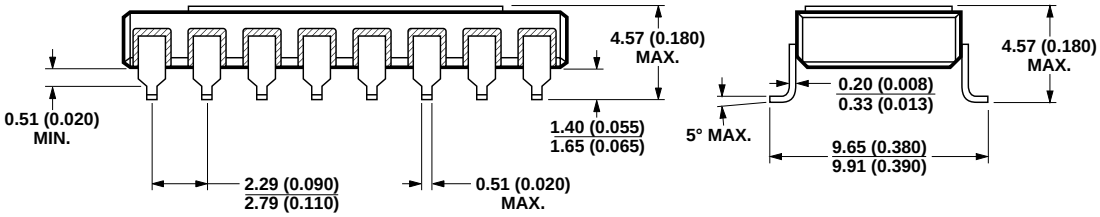
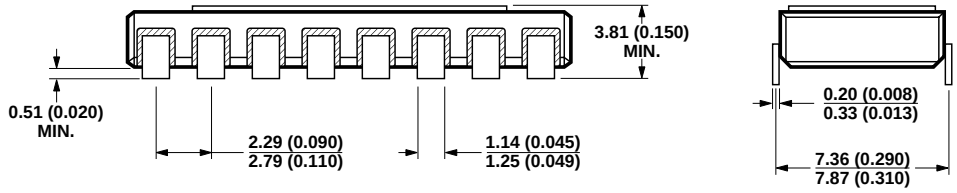
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Device Marking



* QUALIFIED PARTS ONLY

Hermetic Optocoupler Options

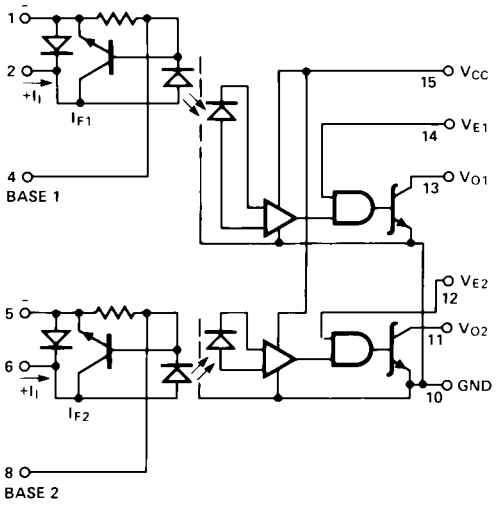
Option	Description
100	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. 
200	Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product. DSCC Drawing part numbers contain provisions for lead finish.
300	Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product. This option has solder dipped leads. 
600	Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product. Contact factory for the availability of this option on DSCC part types. 

Notes: Dimensions in millimeters (inches).
Solder contains lead.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-65	+150	°C	
Operating Temperature	T_A	-55	+125	°C	
Lead Solder Temperature			260 for 10 sec	°C	
Forward Input Current (each channel)	I_I		60	mA	2
Reverse Input Current	I_R		60	mA	
Supply Voltage (1 minute max)	V_{CC}		7.0	V	
Enable Input Voltage (each channel)	V_E		5.5 (not to exceed V_{CC} by more than 500mV)	V	
Output Collector Current (each channel)	I_O		25	mA	
Output Collector Power Dissipation (each channel)	P_O		40	mW	
Output Collector Voltage (each channel)	V_O		7	V	
Total Package Power Dissipation			564	mW	
Input Power Dissipation (each channel)			168	mW	

Schematic



A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 10 AND 15 (SEE NOTE 1).

ESD Classification

(MIL-STD-883, Method 3015)	(▲), Class 1

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level*	I_{IH}	12.5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (@ R_L = 4 kΩ)	N		5	TTL Loads
Operating Temperature	T_A	-55	125	°C

*12.5 mA condition permits at least 20% guardband for optical coupling variation. Initial switching threshold is 10 mA or less.

Electrical Specifications T_A = -55°C to 125°C unless otherwise stated. See note 15.

Parameter	Symbol	Test Conditions	Group A Sub-groups	Limits			Units	Fig.	Note
				Min.	Typ.*	Max.			
High Level Output Current	I_{OH}	V_{CC} = 5.5 V, V_O = 5.5 V I_I = 250 µA, V_E = 2.0 V	1, 2, 3		20	250	µA	3	3
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5 V; I_I = 10 mA V_E = 2.0 V, I_{OL} (Sinking) = 10 mA	1, 2, 3		0.3	0.6	V	1	3
Input Voltage	V_I	I_I = 10 mA	1, 2, 3		2.2	2.6	V	2	3
		I_I = 60 mA			2.35	2.75			
Input Reverse Voltage	V_R	I_R = 10 mA	1, 2, 3		0.8	1.10	V		3
Low Level Enable Current	I_{EL}	V_{CC} = 5.5 V, V_E = 0.5 V	1, 2, 3		-1.45	-2.0	mA		3
High Level Enable Current	I_{EH}	V_{CC} = 5.5 V, V_E = 1.7 V	1, 2, 3			-1.5	mA		3
High Level Enable Voltage	V_{EH}		1, 2, 3	2.0			V		3, 12
Low Level Enable Voltage	V_{EL}		1, 2, 3			0.8	V		3
High Level Supply Current	I_{CCH}	V_{CC} = 5.5 V; I_I = 0, V_E = 0.5 V both channels	1, 2, 3		21	28	mA		
Low Level Supply Current	I_{CCL}	V_{CC} = 5.5 V; I_I = 60 mA, V_E = 0.5 V both channels	1, 2, 3		27	36	mA		
Input-Output Insulation Leakage Current	I_{I-O}	Relative Humidity ≤ 65% t = 5 s, V_{I-O} = 1500 Vdc	1			1	µA		4
Propagation Delay Time to High Output Level	t_{PLH}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA,V_{CC} = 5.0 V	9		55	100	ns	4, 5	3, 5
			10, 11			140			
Propagation Delay Time to Low Output Level	t_{PHL}	R_L = 510 Ω; C_L = 50 pF, I_I = 13 mA, V_{CC} = 5.0 V	9		60	100	ns	4, 5	3, 6
			10, 11			120			
Common Mode Transient Immunity at High Output Level	$\|CM_H\|$	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 510 Ω; I_I = 0 mA, V_{CC} = 5.0 V	9, 10, 11	1000	10,000		V/µs	8, 9	3, 9, 14
Common Mode Transient Immunity at Low Output Level	$\|CM_L\|$	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 510 Ω; I_I = 10 mA, V_{CC} = 5.0 V	9, 10, 11	1000	10,000		V/µs	8, 9	3, 10, 14

*All typical values are at V_{CC} = 5 V, T_A = 25°C.

Typical Specifications

T_A = 25°C, V_{CC} = 5 V

Parameter	Symbol	Typ.	Units	Test Conditions	Fig.	Note
Resistance (Input-Output)	R_{I-O}	10^{12}	Ω	V_{I-O} = 500 V dc		3, 13
Capacitance (Input-Output)	C_{I-O}	1.7	pF	f = 1 MHz		3, 13
Input-Input Insulation Leakage Current	I_{I-I}	0.5	nA	≤ 65% Relative Humidity, V_{I-I} = 500 Vdc, t = 5 s		11
Resistance (Input-Input)	R_{I-I}	10^{12}	Ω	V_{I-I} = 500 Vdc		11
Capacitance (Input-Input)	C_{I-I}	0.55	pF	f = 1 MHz		11
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	35	ns	R_L = 510 Ω, C_L = 15 pF, I_I = 13 mA, V_{EH} = 3 V, V_{EL} = 0 V	6, 7	3, 7
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	35	ns		6, 7	3, 8
Output Rise Time (10-90%)	t_r	30	ns	R_L = 510 Ω, C_L = 15 pF, I_I = 13 mA		3
Output Fall Time (90-10%)	t_f	24	ns			3
Input Capacitance	C_I	60	pF	f = 1 MHz, V_I = 0, PINS 1 to 2 or 5 to 6		3

Notes:

1. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolators should be separate from the bus for any active loads, otherwise additional bypass capacitance may be needed to suppress regenerative feedback via the power supply.
2. Derate linearly at 1.2 mA/°C above T_A = 100°C.
3. Each channel.
4. Device considered a two terminal device: pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.
5. The t_{PLH} propagation delay is measured form the 6.5 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5 mA point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse.
7. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
8. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
9. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state, i.e. V_{OUT} > 2.0 V.
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state, i.e. V_{OUT} < 0.8 V.
11. Measured between adjacent input leads shorted together, i.e. between 1, 2 and 4 shorted together and pins 5, 6 and 8 shorted together.
12. No external pull up is required for a high logic state on the enable input.
13. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10 through 15 shorted together.
14. Parameters shall be tested as part of device initial characterization and after process changes. Parameters shall be guaranteed to the limits specified for all lots not specifically tested.
15. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). Hi-Rel and SMD parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).

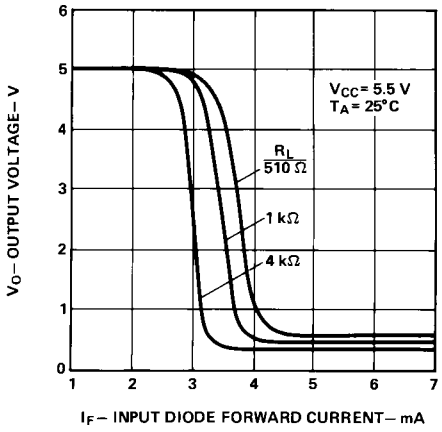


Figure 1. Input-Output Characteristics.

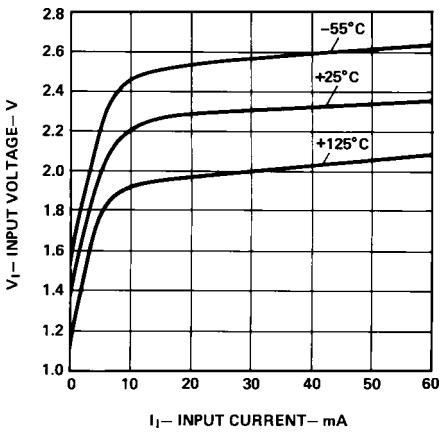


Figure 2. Input Characteristics.

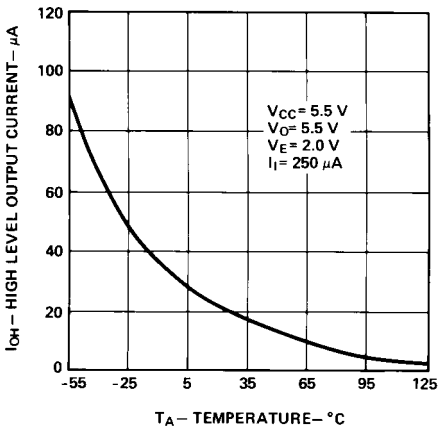


Figure 3. High Level Output Current vs. Temperature.

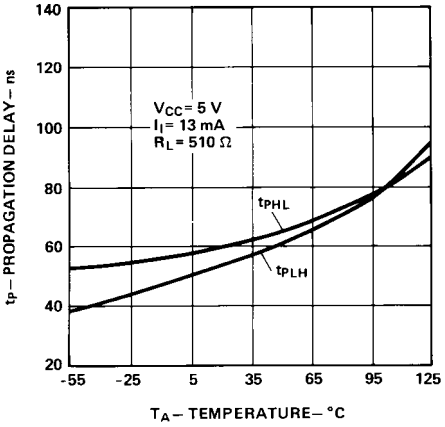


Figure 4. Propagation Delay vs. Temperature.

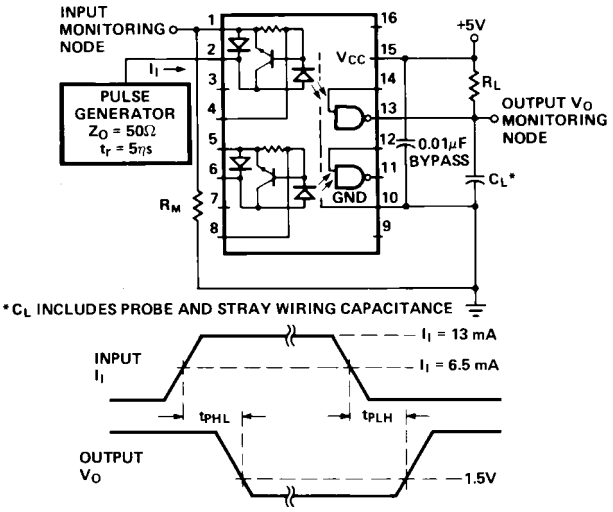


Figure 5. Test Circuit for t_{PHL} and t_{PLH}.

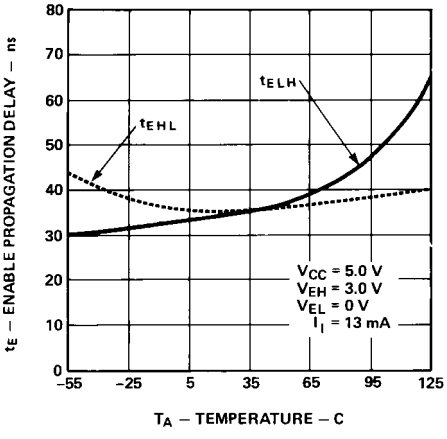


Figure 6. Enable Propagation Delay vs. Temperature.

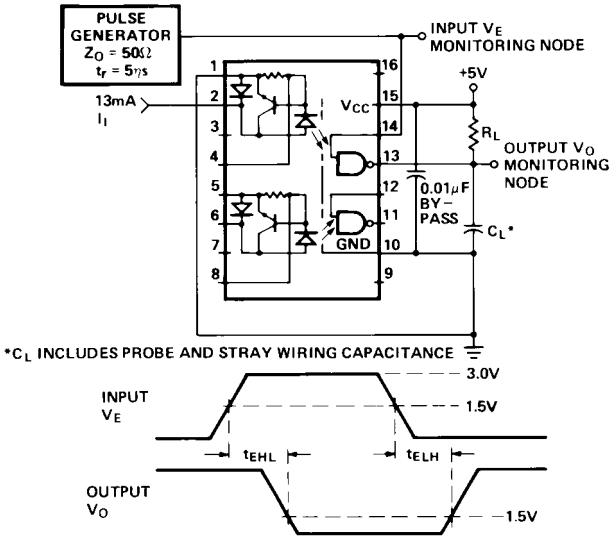


Figure 7. Test Circuit for t_{EHL} and t_{ELH}.

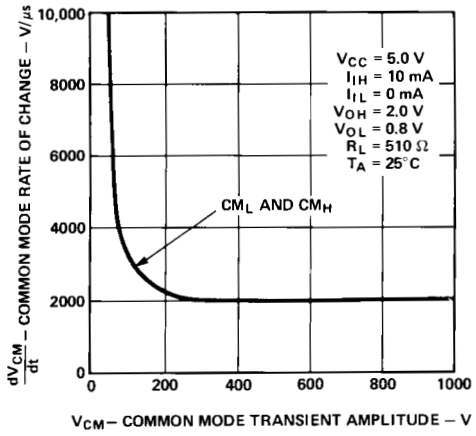


Figure 8. Typical Common Mode Transient Immunity.

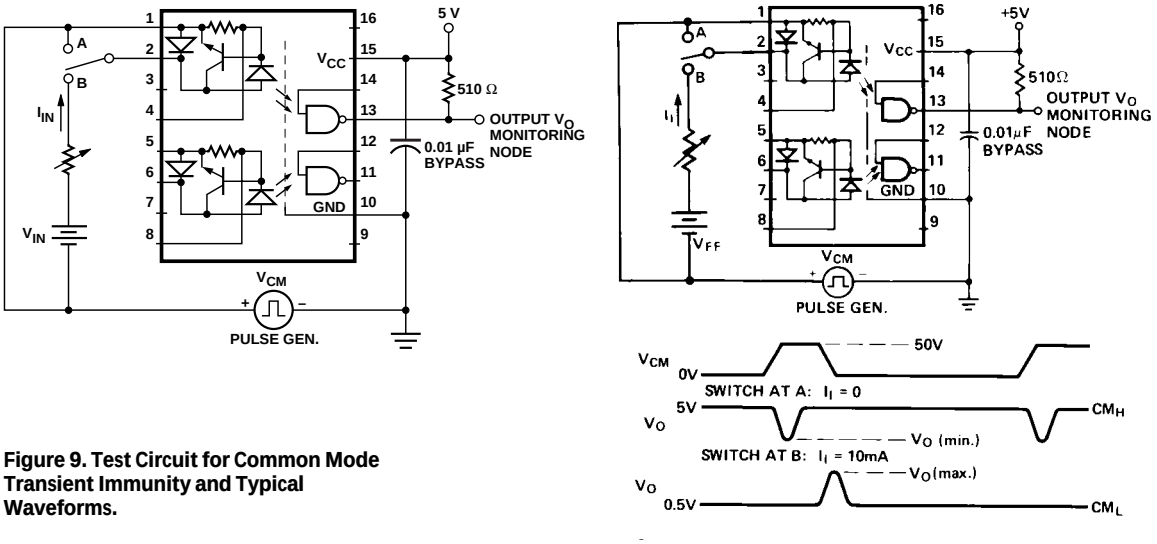


Figure 9. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

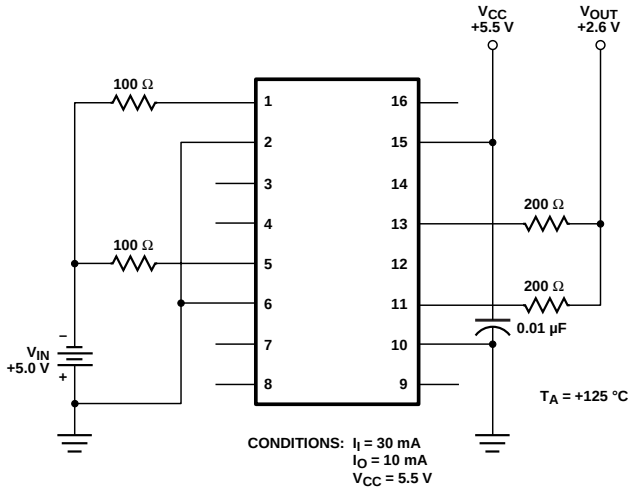
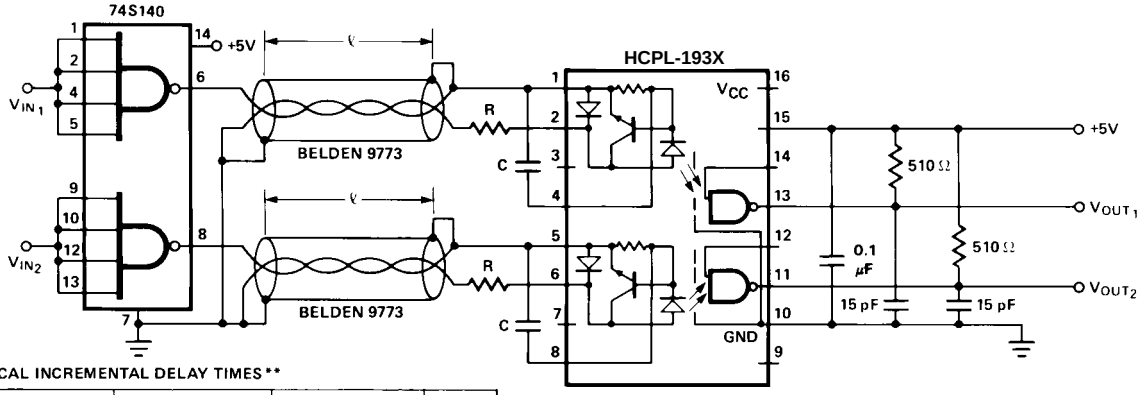


Figure 10. Burn In Circuit.

Application Circuits*

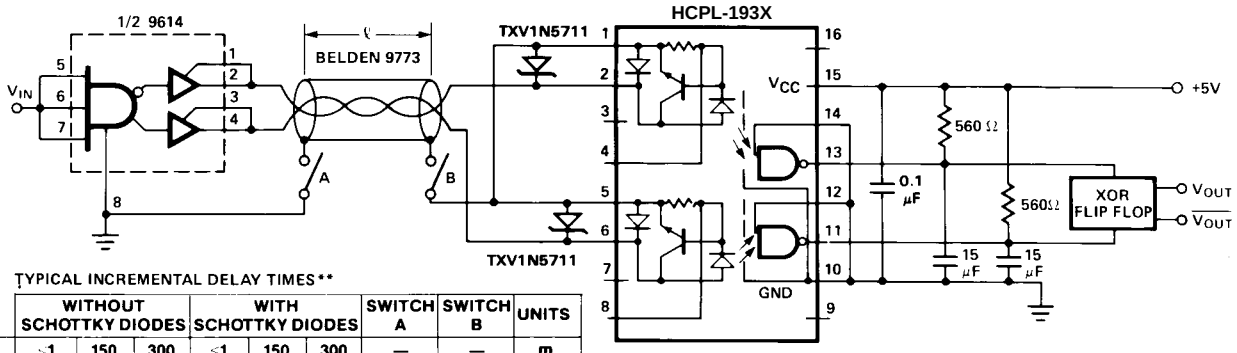


TYPICAL INCREMENTAL DELAY TIMES**

	R = 0, C = OPEN			R =33Ω, C = OPEN			R=33Ω, C = 390pF			UNITS
ℓ	<1	150	300	<1	150	300	<1	150	300	m
t_{PHL}	42	27	121	43	47	171	28	37	146	nsec
t_{PLH}	31	121	296	31	31	71	26	11	46	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure A_1. Polarity Non-Reversing.

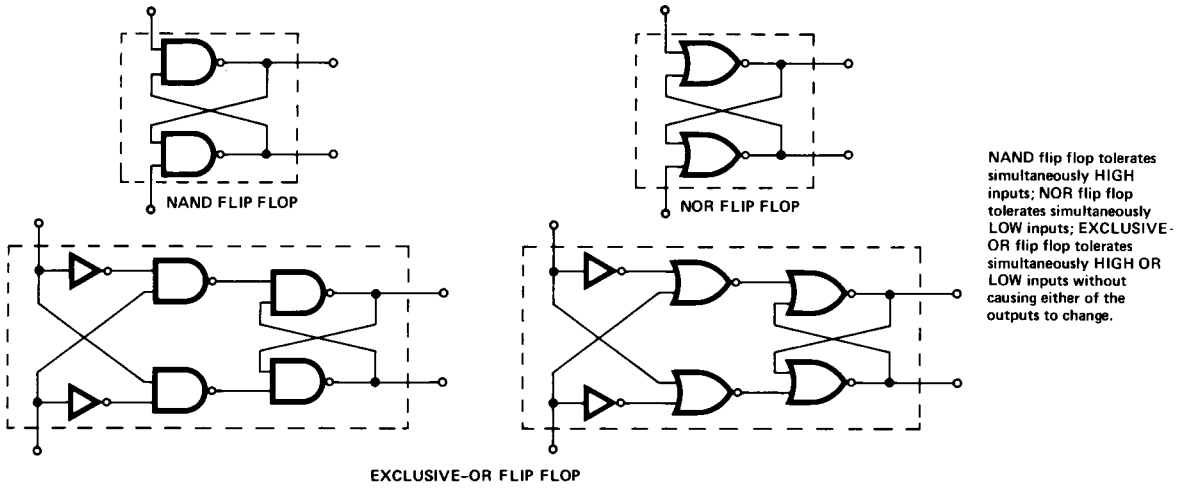


TYPICAL INCREMENTAL DELAY TIMES**

	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	150	300	<1	150	300	—	—	m
tp	112	455	820	78	365	700	OPEN	OPEN	nsec
	52	410	730	54	305	580	OPEN	CLOSED	nsec
	52	410	490	54	395	490	CLOSED	CLOSED	nsec

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS
USING 1/3 74LS04 INVERTERS AND 74LS00 QUAD NAND

Figure A_2. Polarity Reversing, Split Phase.



*FOR A DESCRIPTION OF THESE CIRCUITS SEE HCPL-2602 DATA SHEET.

Figure A_3. Flop-Flop Configurations.

MIL-PRF-38534 Class H, Class K, and DSCC SMD Test Program

Avago Technologies' Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Class H and K. Class H and Class K devices are also in compliance with DSCC drawing 5962-89572.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

5968-9401E June 19, 2007

AVAGO TECHNOLOGIES