晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AT-160240B
APPROVED BY	
DATE	

AMPIRE CO., LTD.
TOWER A, 4F, No.114, Sec. 1, HSIN-TAI 5th RD., HIS-CHIH,
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APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Contents
2001/11/20	New Release

1 FEATURES

(1) Display format : 160 × 240 dot-matrix , 1/160 duty, portrait display format.

(2) Construction : FSTN LCD, TAB IC and FPC.

(3) Option : Touch panel, EL backlight.

(4) Common driver is NT7701 and Segment is NT7702, or equivalent one.

(5) 3.3V for driver IC. LCD bias voltage is supplied by end user.

(6) Extended temperature type.

2 MECHANICAL DATA

Parameter	Stand Value	Unit
Dot size	0.31(W) × 0.295(H)	Mm
Dot pitch	0.325(W) × 0.31(H)	Mm
Active area	51.985 (W) × 74.385 (H)	Mm
Viewing area	58.9(W) × 77.8(H)	Mm
LCD size	67.0(W) × 85.1(H)	Mm
Module size	70.0(W) × 90.5(H) × 4.8 max (T)	Mm

3 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Logic Circuit Supply Voltage	VDD-VSS	-0.3	7.0	V
LCD Driving Voltage	VEE-VSS	-0.3	26.0	V
Input Voltage	V_I	-0.3	VDD+0.3	V
Operating Temp.	T_{OP}	-10	60	°C
Storage Temp.	T_{STG}	-20	70	°C

4 ELECTRO-OPTICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
----- Electronic Characteristics -----							
Logic Circuit Supply Voltage	VDD-VSS	--	2.7	3.3	5.5	V	
LCD Driving Voltage	VEE-VSS	-10°C		21.9	--	V	
		-5°C		21.8			
		0°C		21.7			
		5°C		21.5			
		10°C		21.3			
		15°C		21.2			
		20°C		20.9			
		25°C	20.7	20.8	21.2		
		50°C		19.6			
		70°C		19.0			
Input Voltage	VIH	--	0.8 VDD	--	VDD	V	
	VIL	--	VSS	--	0.2 VDD	V	
Logic Supply Current	IDD	VDD = 3.3V	--	2	--	mA	
----- Optical Characteristics -----							
Contrast	CR	25°C	6	8	--		Note 1
Rise Time	tr	25°C	--	100	150	ms	Note 2
Fall Time	tf	25°C	--	300	350	ms	
Viewing Angle Range	θ f	25°C & CR≥2	37	37	38	Deg.	Note 3
	θ b		30	30	30		
	θ l		37	38	40		
	θ r		35	37	39		
Frame Frequency	fF	25°C	--	64	--	Hz	

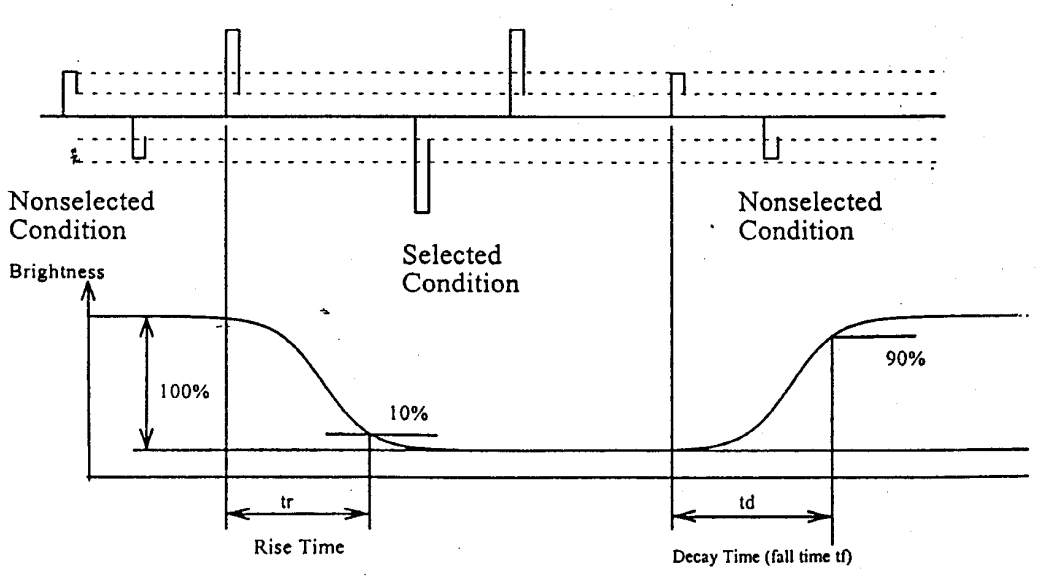
4.1 EL Back-light Electrical Specification

Parameter	Specification	Unit
Color	Blue-Green	-
Voltage	Vrms = 100	V(AC)
Frequency	Sine Wave = 400	Hz
Current Density	0.12	mA / cm^2
Bare EL Initial Brightness	60	cd / m^2
LCM Initial Brightness	20	cd / m^2
Life time	2,000	Hrs

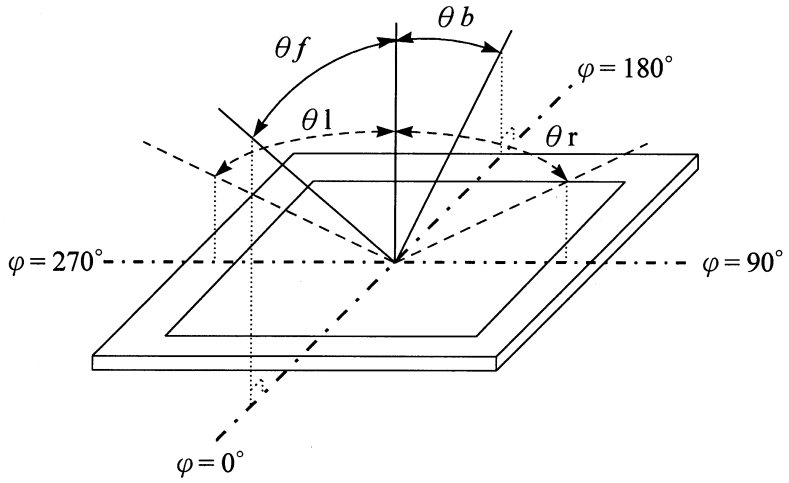
(NOTE 1) Contrast ratio :

CR = (Brightness in OFF state) / (Brightness in ON state)

(NOTE 2) Response time :



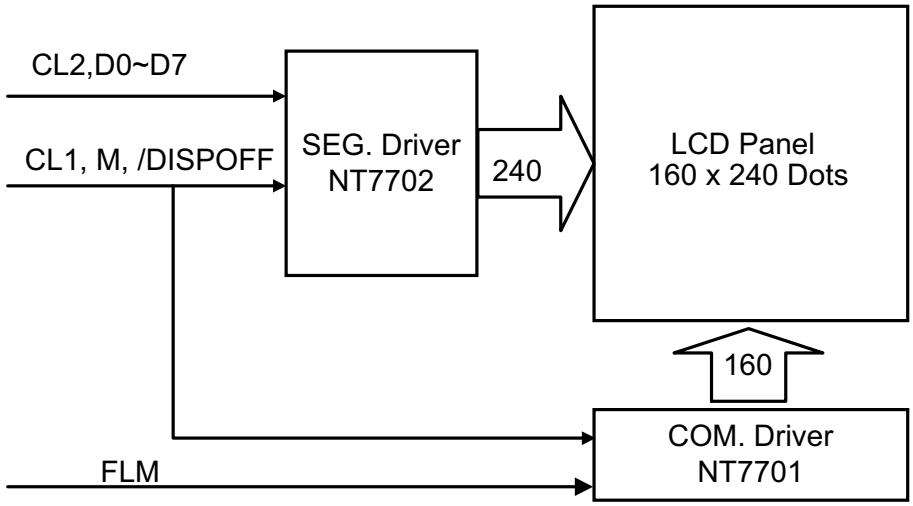
(NOTE 3) Viewing angle



4.2 Touch Panel Electrical Specification

Parameter	Specification	Condition
ON Resistance	260 Ω ~ 1040 Ω	X Axis
	160 Ω ~ 640 Ω	Y Axis
Insulating Resistance	More than 20MΩ	DC 25 V
Chattering	Less Than 10 ms	DC 5V, Load of resistance(1mA), switching Time 2m/sec
Endurable Voltage	25 V for 1 min	

5 BLOCK DIAGRAM



6 PIN CONNECTIONS

No.	Symbol	Function
1	FLM	First Line Marker
2	V1	Common non-select level
3	V4	
4	VDD	Supply Voltage for Logic (+3.3V)
5	VEE	Power Supply for LCD drive (+V)
6	CL1	Data Latch Clock
7	VSS	Ground (0V)
8	CL2	Data Shift Clock
9	M	Alternate signal for LCD driving waveform
10	/DISPOFF	Display Off Control
11-18	D0-D7	Data Bus Line
19	VSS	Ground (0V)
20	V2	Segment non-select level
21	V3	
22	VSS	Ground (0V)
23	VEL1	EL power supply
24	VEL2	EL power supply

7 TIMING CHARACTERISTICS

AC Characteristics

Segment Mode 1 (V_{SS}=V_S=0V, V_{DD}= 4.5~5.5V, V_O=15 to 30 V, and T_A=-20 to +85°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	50	-		ns	tr, tf≦10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	15	-		ns	
Shift clock "L" pulse width	t_{WCKL}	15	-		ns	
Data setup time	t_{DS}	10	-		ns	
Data hole time	t_{DH}	12	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	15	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	30	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	25	-		ns	
Latch pulse fall to Shift clock rise time	t_{LH}	25	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	10	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		µs	
Output delay time (1)	t_D		-	30	ns	CL=15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	µs	CL=15pF
Output delay time (3)	t_{pd3}		-	1.2	µs	CL=15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKII} -t_{WCKI})/2 is maximum in the case of high speed operation.

Segment Mode 2 (V_{SS}=V_5=0V, V_{DD}= 3.0~4.5V, V_0=15 to 30 V, and T_A=-20 to +85°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	66	-		ns	tr, tf≦10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	23	-		ns	
Shift clock "L" pulse width	t_{WCKL}	23	-		ns	
Data setup time	t_{DS}	15	-		ns	
Data hole time	t_{DH}	23	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	30	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	50	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	30	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	30	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		µs	
Output delay time (1)	t_D		-	41	ns	CL=15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	µs	CL=15pF
Output delay time (3)	t_{pd3}		-	1.2	µs	CL=15pF

Note

1. Take the cascade connection into consideration.
2. (t_{CK}-t_{WCKH} -t_{WCKL})/2 is maximum in the case of high speed operation.

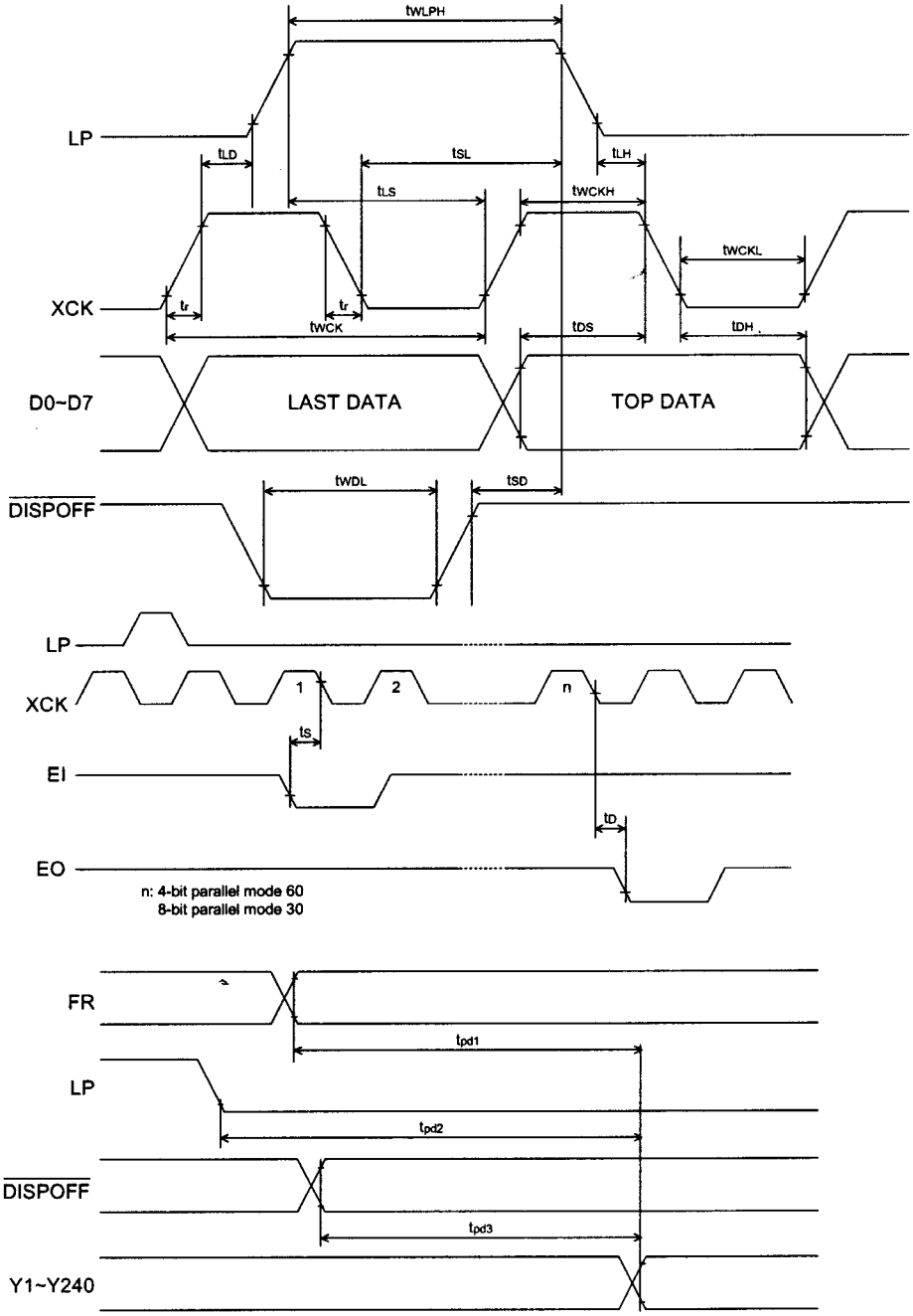
Segment Mode 3 (V_{SS}=V_5=0V, V_{DD}= 2.5~3.0V, V_0=15 to 30 V, and T_A=-20 to +85°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	t_{WCK}	82	-		ns	tr, tf≦10ns, Note 1
Shift clock "H" pulse width	t_{WCKH}	28	-		ns	
Shift clock "L" pulse width	t_{WCKL}	28	-		ns	
Data setup time	t_{DS}	20	-		ns	
Data hole time	t_{DH}	23	-		ns	
Latch pulse "H" pulse width	t_{WLPH}	30	-		ns	
Shift clock rise to Latch pulse rise time	t_{LD}	0	-		ns	
Shift clock fall to Latch pulse fall time	t_{SL}	65	-		ns	
Latch pulse rise to Shift clock rise time	t_{LS}	30	-		ns	
Latch pulse fall to Shift clock fall time	t_{LH}	30	-		ns	
Input signal rise time	t_r		-	50	ns	Note 2
Input signal fall time	t_f		-	50	ns	Note 2
Enable setup time	t_S	15	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t_{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t_{WDL}	1.2	-		µs	
Output delay time (1)	t_D		-	57	ns	CL=15pF
Output delay time (2)	t_{pd1}, t_{pd2}		-	1.2	µs	CL=15pF
Output delay time (3)	t_{pd3}		-	1.2	µs	CL=15pF

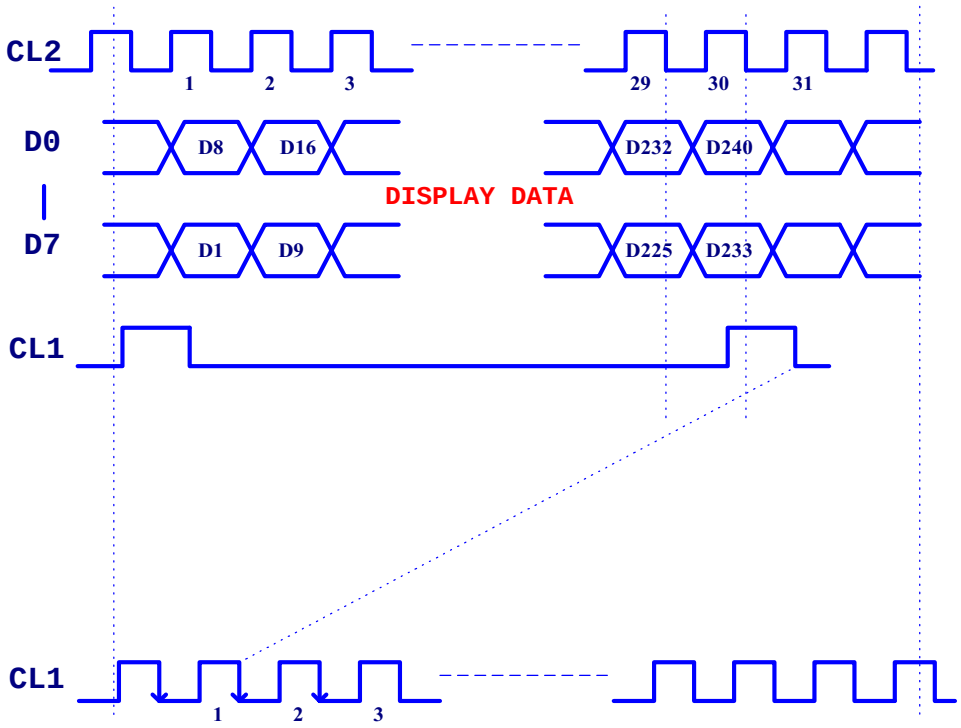
Note

3. Take the cascade connection into consideration.
4. (t_{CK}-t_{WCKH} -t_{WCKL})/2 is maximum in the case of high speed operation.

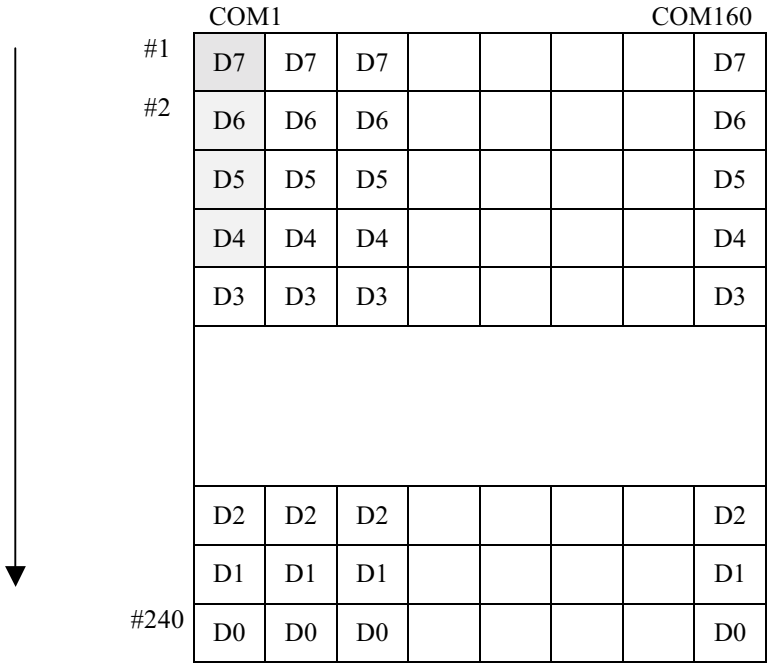
Timing waveform of Segment Mode



7.1 Controller Interface Timing Chart



7.2 Display Data Format

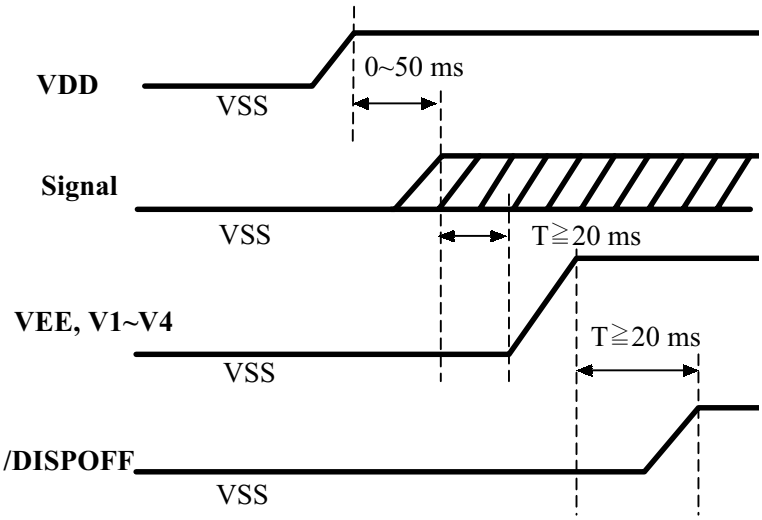


Portrait Display Type (Top View)

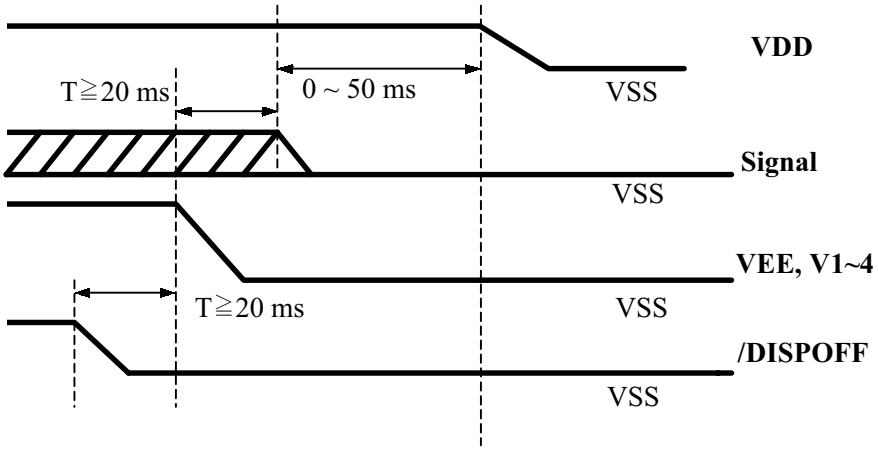
7.3 Power ON/OFF Sequence

Please maintain the blow sequence when turning on and off the power supply of the module. If /DISPOFF is supplied to the module while internal alter signal for LCD driving (M) is unstable, DC component will be supplied to the LCD panel. This may cause damage the LCD module.

POWER ON SEQUENCE



POWER OFF SEQUENCE



8 QUALITY AND RELIABILITY

8.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 5°C

Humidity : 60 ± 25% RH.

8.2 SAMPLING PLAN

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

8.3 ACCEPTABLE QUALITY LEVEL

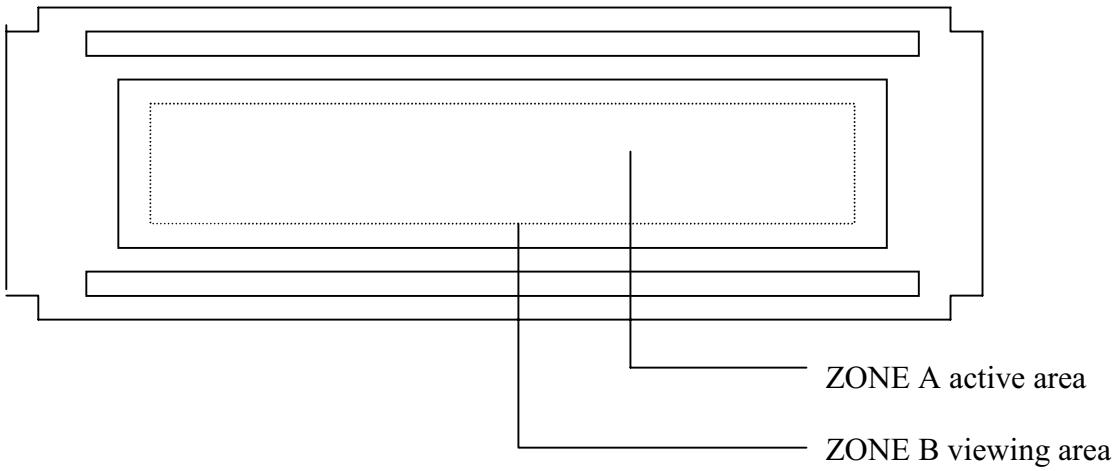
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

8.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.

8.5 INSPECTION QUALITY CRITERIA

Item	Description of defects			Class of Defects	Acceptable level (%)
Function	Short circuit or Pattern cut			Major	0.65
Dimension	Deviation from drawings			Major	1.5
Black spots	Ave . dia . D	area A	area B	Minor	2.5
	D≤0.2	Disregard			
	0.2<D≤0.3	3	4		
	0.3<D≤0.4	2	3		
	0.4<D	0	1		
Black lines	Width W, Length L	A	B	Minor	2.5
	W≤0.03	disregard			
	0.03<W≤0.05	3	4		
	0.05<W≤0.07 , L≤3.0	1	1		
	See line criteria				
Bubbles in polarizer	Average diameter D 0.2 < D < 0.5 mm for N = 4 , D > 0.5 for N = 1			Minor	2.5
Color uniformity	Rainbow color or newton ring.			Minor	2.5
Glass Scratches	Obvious visible damage.			Minor	2.5
Contrast ratio	See note 1			Minor	2.5
Response time	See note 2			Minor	2.5
Viewing angle	See note 3			Minor	2.5



8.6 RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	60 ± 3°C , t=96 hrs	
Low Temperature Operation	-10 ± 3°C , t=96 hrs	
High Temperature Storage	70 ± 3°C , t=96 hrs	1,2
Low Temperature Storage	-20 ± 3°C , t=96 hrs	1,2
Humidity Test	40°C , Humidity 90%, 96 hrs	1,2
Thermal Shock Test	-20°C (30 min.) ~ 25°C (5 min.) ~ 70°C (30 min.) (1 cycle) Total 5 cycle	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

9 HANDLING PRECAUTIONS

(1) A LCD module is a fragile item and should not be subjected to strong mechanical shocks.

(2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in color.

(3) Under no circumstances should the position of the bezel tabs or their shape be modified.

(4) Do not modify the display PCB in either shape or positioning of components.

(5) Do not modify or move location of the zebra or heat seal connectors.

(6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.

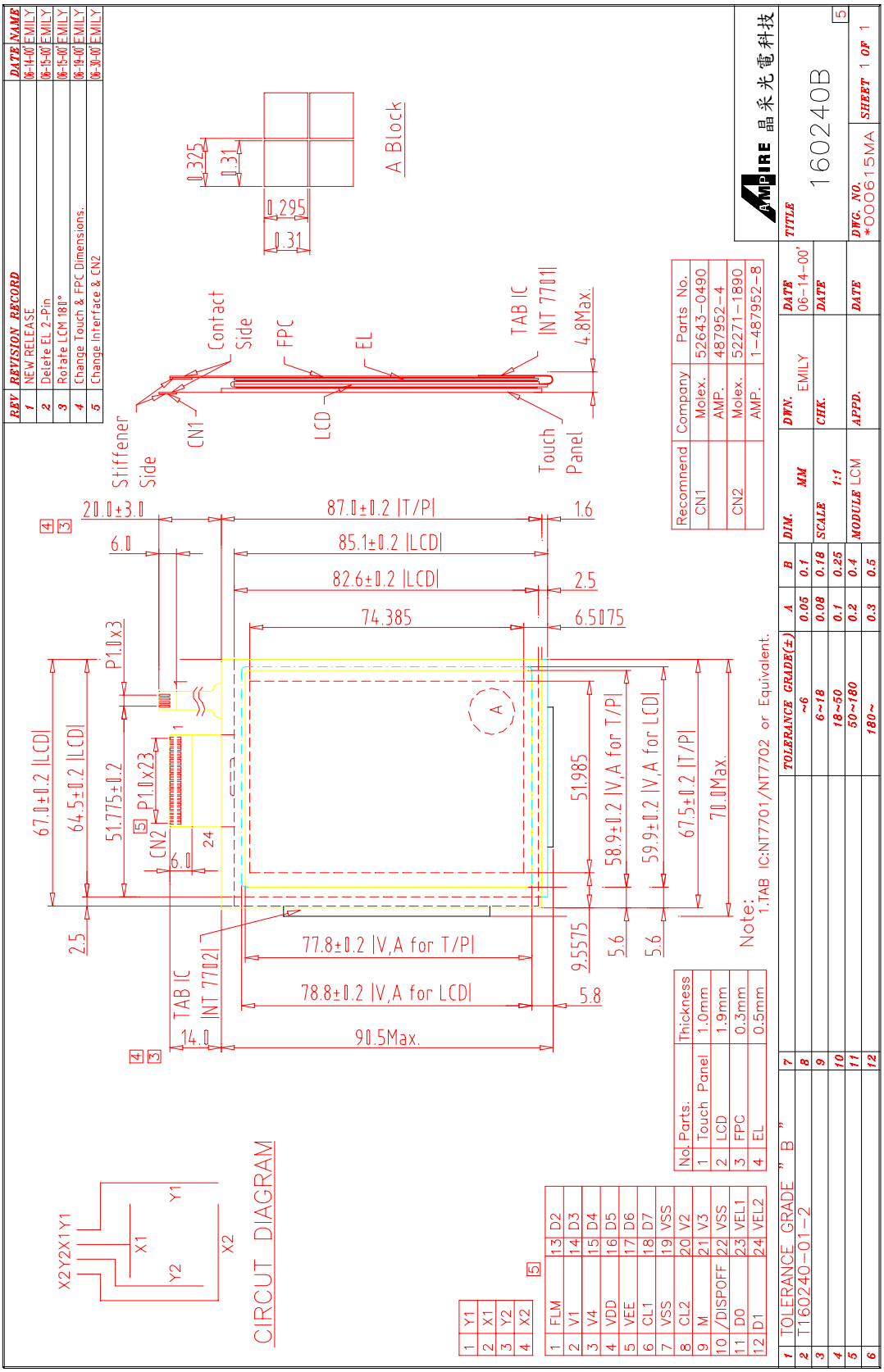
(7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.

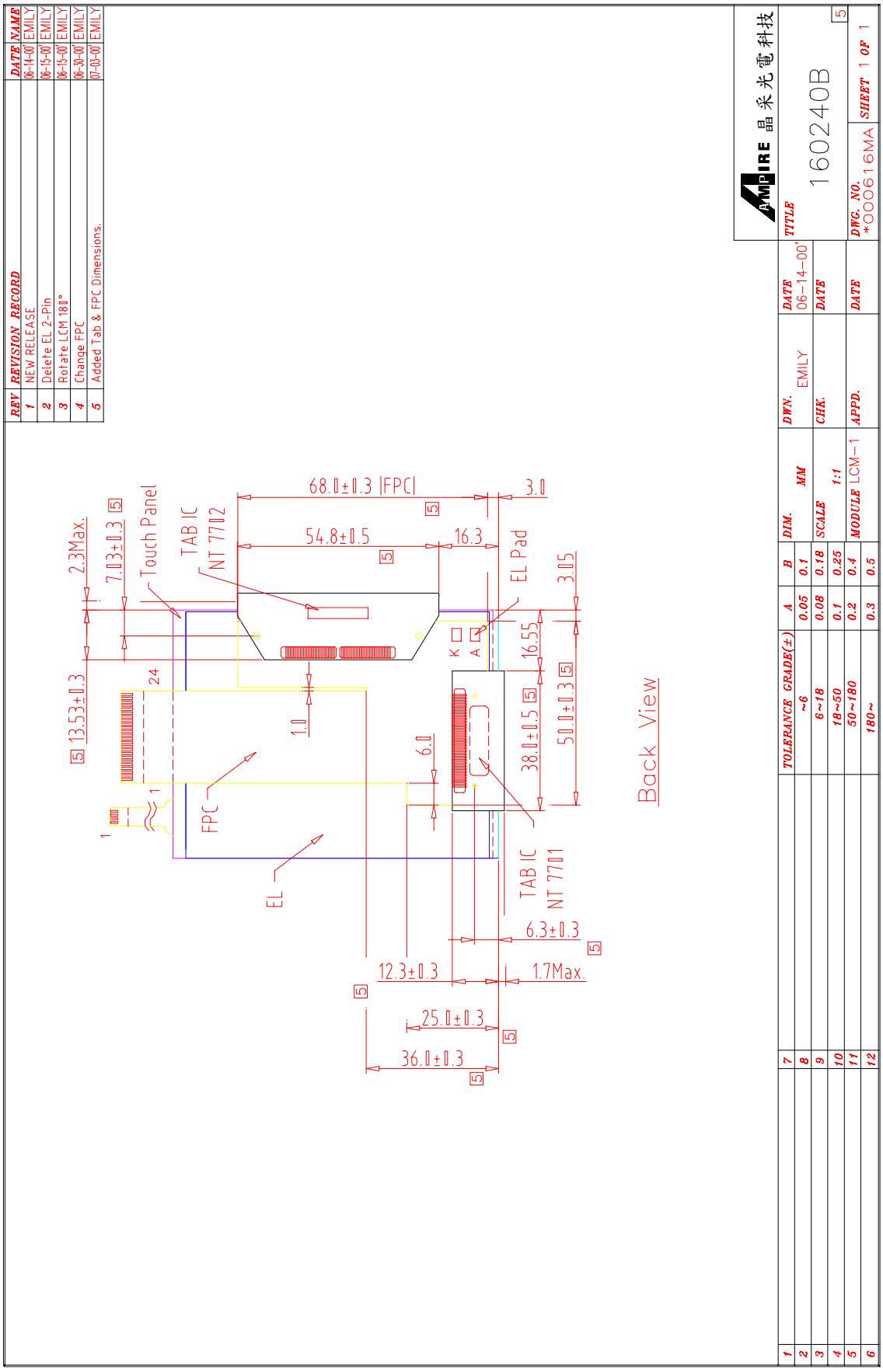
(8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.

(9) Prior to initial power up input signals should not be applied.

(10) Protect the module against static electricity and observe appropriate anti-static precautions.

10 OUTLINE DIMENSION




REV
REVISION RECORD
DATE
NAME
1 NEW RELEASE 06-14-00' EMILY
2 Delete EL 2-Pin 06-15-00' EMILY
3 Rotate LCM 180° 06-15-00' EMILY
4 Change FPC 06-30-00' EMILY
5 Added Tab & FPC Dimensions. 07-03-00' EMILY
AMPIRE 晶采光電科技
TITLE
160240B
DWG. NO.
*000616MA
SHEET 1 OF 1
DWN. EMILY
DATE 06-14-00'
CHK.
APPD.
DIM. MM
SCALE 1:1
MODULE LCM-1
TOLERANCE GRADE(±)
~6
6~18
18~50
50~180
180~
A 0.05 0.08 0.1 0.2 0.3
B 0.1 0.18 0.25 0.4 0.5
68.0±0.3 (FPC)
3.0
54.8±0.5
16.3
EL Pad
3.05
2.3Max.
7.03±0.3
Touch Panel
TAB IC
NT 7702
13.53±0.3
24
1.0
16.55
50.0±0.3
38.0±0.5
6.0
FPC
EL
TAB IC
NT 7701
6.3±0.3
12.3±0.3
1.7Max.
25.0±0.3
36.0±0.3
Back View