

## 3.3V CMOS OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS, 5 VOLT TOLERANT I/O AND BUS-HOLD

### IDT74LVCH245A

## **FEATURES**:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Vcc = 3.3V ± 0.3V, Normal Range
- Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (0.4 w W typ. static)
- · Rail-to-rail output swing for increased noise margin
- All inputs, outputs, and I/O are 5V tolerant
- · Supports hot insertion
- · Available in SOIC, SSOP, QSOP, and TSSOP packages

### **DRIVE FEATURES:**

- · High Output Drivers: ±24mA
- · Reduced system switching noise

### **APPLICATIONS:**

- 5V and 3.3V mixed voltage systems
- · Data communication and telecommunication systems

## **DESCRIPTION:**

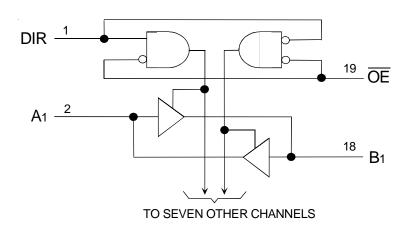
The LVCH245A octal bus transceiver is built using advanced dual metal CMOS technology. The device is designed for asynchronous communication between data buses. Data is transmitted from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction-control (DIR) input. The output-enable  $(\overline{OE})$  input can be used to disable the device so the buses are effectively isolated.

The LVCH245A has been designed with a  $\pm 24$ mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The LVCH245A has "bus-hold" which retains the inputs' last state whenever the input goes to a high-impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

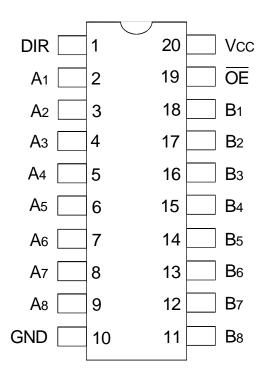
Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device as a translator in a mixed 3.3 V/5 V system environment.

## FUNCTIONAL BLOCK DIAGRAM



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### **PIN CONFIGURATION**



SOIC/ SSOP/ QSOP/ TSSOP TOP VIEW

## ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +6.5	V
Tstg	Storage Temperature	-65 to +150	°C
Іоит	DC Output Current	-50 to +50	mA
lik lok	Continuous Clamp Current, VI < 0 or Vo < 0	<b>-</b> 50	mA
lcc Iss	Continuous Current through each Vcc or GND	±100	mA

#### NOTE:

 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Тур.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
Соит	Output Capacitance	Vout = 0V	5.5	8	pF
Cı/o	I/O Port Capacitance	VIN = 0V	6.5	8	pF

#### NOTE:

1. As applicable to the device type.

## **PIN DESCRIPTION**

Pin Names	Description	
ŌĒ	Output Enable Input (Active LOW)	
DIR	Direction Control Input	
Ax	Data Inputs <sup>(1)</sup>	
Вх	Data Outputs	

#### NOTE:

1. These pins have "Bus-Hold". All other pins are standard inputs, outputs, or I/Os.

## FUNCTION TABLE(1)

Inp	uts	
ŌĒ	DIR	Outputs
L	L	Bus B Data to Bus A
L	Н	Bus A Data to Bus B
Н	Х	Z

#### NOTES:

1. H = HIGH Voltage Level

X = Don't Care

L = LOW Voltage Level

Z = High-Impedance

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $TA = -40^{\circ}C$  to  $+85^{\circ}C$ 

Symbol	Parameter	Test Co	onditions	Min.	Typ. <sup>(1)</sup>	Max.	Unit
VIH	Input HIGH Voltage Level	Vcc = 2.3V to 2.7V		1.7	_	_	V
		Vcc = 2.7V to 3.6V		2	_	_	
VIL	Input LOW Voltage Level	Vcc = 2.3V to 2.7V		_	_	0.7	V
		Vcc = 2.7V to 3.6V		_	_	0.8	
Іін	Input Leakage Current	Vcc = 3.6V	VI = 0 to 5.5V	_	_	±5	μΑ
lıL							
lozh	High Impedance Output Current	Vcc = 3.6V	Vo = 0 to 5.5V	_	_	±10	μΑ
lozl	(3-State Output pins)						
loff	Input/Output Power Off Leakage	$VCC = 0V$ , $VIN or VO \le 5.5V$		_	_	±50	μΑ
Vik	Clamp Diode Voltage	VCC = 2.3V, IIN = -18mA		_	-0.7	-1.2	V
VH	Input Hysteresis	Vcc = 3.3V		_	100	_	mV
ICCL	Quiescent Power Supply Current	Vcc = 3.6V	VIN = GND or VCC	_	_	10	μΑ
ICCH ICCZ			$3.6 \le VIN \le 5.5V^{(2)}$	+ -	_	10	
Δlcc	Quiescent Power Supply Current Variation	One input at Vcc - 0.6V, other	inputs at Vcc or GND	_	_	500	μΑ

#### NOTES:

- 1. Typical values are at Vcc = 3.3V, +25°C ambient.
- 2. This applies in the disabled state only.

## **BUS-HOLD CHARACTERISTICS**

Symbol	Parameter <sup>(1)</sup>	Test Conditions		Min.	Typ. <sup>(2)</sup>	Max.	Unit
Івнн	Bus-Hold Input Sustain Current	Vcc = 3V	VI = 2V	<b>- 75</b>	_	_	μΑ
IBHL			VI = 0.8V	75	_	_	
Івнн	Bus-Hold Input Sustain Current	Vcc = 2.3V	VI = 1.7V	_	_	_	μΑ
IBHL			VI = 0.7V	_	_	_	
Івнно	Bus-Hold Input Overdrive Current	Vcc = 3.6V	VI = 0 to 3.6V	_	_	±500	μΑ
Івньо							

#### NOTES:

- 1. Pins with Bus-Hold are identified in the pin description.
- 2. Typical values are at Vcc = 3.3V, +25°C ambient.

## **OUTPUT DRIVE CHARACTERISTICS**

Symbol	Parameter	Test Con	ditions <sup>(1)</sup>	Min.	Max.	Unit
Vон	Output HIGH Voltage	Vcc = 2.3V to 3.6V	IOH = - 0.1mA	Vcc-0.2	_	V
		Vcc = 2.3V	IOH = -6mA	2	_	
		Vcc = 2.3V	IOH = - 12mA	1.7	_	
		Vcc = 2.7V		2.2	_	
		Vcc = 3V		2.4	_	
		Vcc = 3V	IOH = - 24mA	2.2	_	
Vol	Output LOW Voltage	Vcc = 2.3V to 3.6V	IoL = 0.1mA		0.2	V
		Vcc = 2.3V	IoL = 6mA	_	0.4	
			IoL = 12mA	_	0.7	
		Vcc = 2.7V	IoL = 12mA	_	0.4	
		VCC = 3V	Iol = 24mA	_	0.55	

#### NOTE:

## OPERATING CHARACTERISTICS, Vcc = 3.3V ± 0.3V, Ta = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per Transceiver Outputs enabled	CL = 0pF, f = 10Mhz	47	pF
CPD	Power Dissipation Capacitance per Transceiver Outputs disabled		2	

## SWITCHING CHARACTERISTICS(1)

		Vcc =	2.7V	Vcc = 3.3	V ± 0.3V	
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
tplH	Propagation Delay	_	7.3	1.5	6.3	ns
tphl.	Ax to Bx, Bx to Ax					
tpzh	Output Enable Time	_	9.5	1.5	8.5	ns
tpzl	OE to Ax or Bx					
tphz	Output Disable Time	_	8.5	1.7	7.5	ns
tplz	OE to Ax or Bx					
tsk(o)	Output Skew <sup>(2)</sup>	_	_	_	1	ns

#### NOTES:

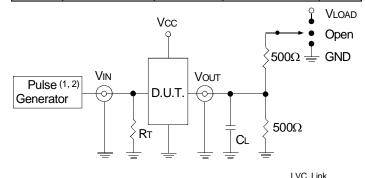
- 1. See TEST CIRCUITS AND WAVEFORMS. TA =  $-40^{\circ}$ C to +  $85^{\circ}$ C.
- 2. Skew between any two outputs of the same package and switching in the same direction.

<sup>1.</sup> VIH and VIL must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate Vcc range. TA = - 40°C to + 85°C.

# TEST CIRCUITS AND WAVEFORMS

### **TEST CONDITIONS**

Symbol	$Vcc^{(1)} = 3.3V \pm 0.3V$	Vcc <sup>(1)</sup> = 2.7V	Vcc <sup>(2)</sup> =2.5V±0.2V	Unit
VLOAD	6	6	2 x Vcc	V
VIH	2.7	2.7	Vcc	V
VT	1.5	1.5	Vcc / 2	V
VLZ	300	300	150	mV
VHZ	300	300	150	mV
CL	50	50	30	pF



Test Circuit for All Outputs

#### **DEFINITIONS:**

CL = Load capacitance: includes jig and probe capacitance.

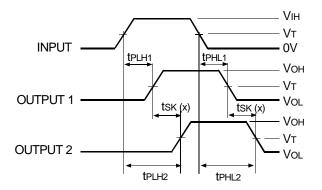
RT = Termination resistance: should be equal to ZouT of the Pulse Generator.

#### NOTES:

- 1. Pulse Generator for All Pulses: Rate  $\leq$  10MHz; tr  $\leq$  2.5ns; tr  $\leq$  2.5ns.
- 2. Pulse Generator for All Pulses: Rate  $\leq$  10MHz; tF  $\leq$  2ns; tR  $\leq$  2ns.

## **SWITCH POSITION**

Test	Switch
Open Drain Disable Low Enable Low	VLOAD
Disable High Enable High	GND
All Other Tests	Open

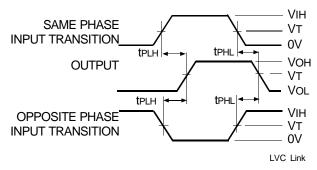


tSK(x) = |tPLH2 - tPLH1| or |tPHL2 - tPHL1|

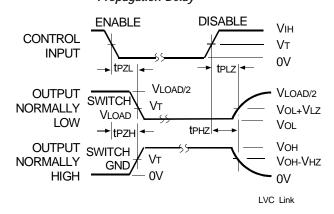
Output Skew - tsk(x)

#### NOTES:

- 1. For tsk(o) OUTPUT1 and OUTPUT2 are any two outputs.
- 2. For tsk(b) OUTPUT1 and OUTPUT2 are in the same bank.



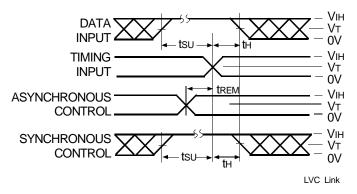
### Propagation Delay



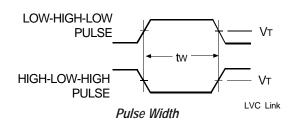
#### **Enable and Disable Times**

#### NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

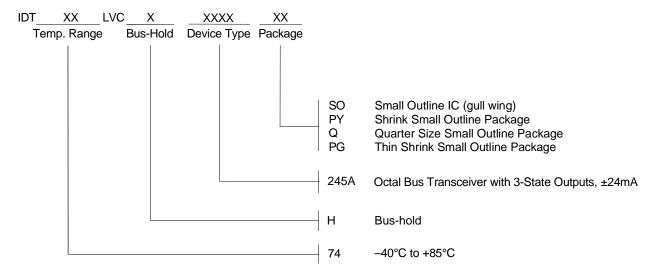


Set-up, Hold, and Release Times



LVC Link

## ORDERING INFORMATION





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### for SALES:

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