

AD7709-SPECIFICATIONS¹

($V_{DD} = +3V$ or $+5.0V$, $REFIN(+) = +2.5V$; $REFIN(-) = 0V$;
 $XTAL1/XTAL2 = 32$ kHz Crystal;
 All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	B Grade	Units	Test Conditions
Output Update Rate	5.4 105	Hz min. Hz max.	0.021Hz (0.732msec.) increments
No Missing Codes	16	bits min.	
Resolution	13 16	bits pk-pk bits pk-pk	+20mV range, 20Hz Update Rate +2.56V range, 20Hz Update Rate
Output Noise and Update Rates	See Tables Below in ADC Description		
Integral Nonlinearity	15	ppm of FSR max.	
Offset Error	TBD		
Offset Error Drift Vs Temp	10	nV/°C typ.	
Offset Error Drift Vs Time	TBD	nV/1000 Hours typ.	
Gain Error	TBD		
Gain Error Drift Vs Temp	1	ppm/°C typ.	
Gain Error Drift Vs Time	TBD	ppm/1000 Hours typ.	
Power Supply Rejection(PSR)	90 90	dB min. dB min.	Input Range = $\pm 20mV$ Input Range = $\pm 2.56V$
Common Mode Rejection(CMR)			
On AIN	90	dB min.	At DC, Range = $\pm 20mV$
On AIN	90	dB min.	At DC, Range = $\pm 2.56V$
On REFIN	90	dB min.	At DC, Range = $\pm 20mV$
On REFIN	90	dB min.	At DC, Range = $\pm 2.56V$
Analog Input Current			
DC Bias Current	1	nA max.	
DC Bias Current Drift	TBD	nA typ.	
DC Offset Current	TBD	nA typ.	
DC Offset Current Drift	TBD	nA typ.	
REFERENCE INPUTS (REFIN1& REFIN2)			
Normal Mode			
50Hz/60Hz Rejection	60	dB min.	
Reference DC Input Current	TBD	μA typ.	
REFIN(+) to REFIN(-) Voltage	+2.5V	nom.	REFIN refers to both REFIN1 and REFIN2
REFIN(+) to REFIN(-) Range	+1 V_{DD}	V min. V max.	
REFIN Common Mode Range	GND-30mV $V_{DD}+30mV$	V min. V max.	
REFIN Common Mode			
50/60Hz Rejection	TBD	dB min.	
ANALOG INPUTS			
Normal Mode 50Hz/60Hz Rejection	60	dB min.	50/60Hz $\pm 1Hz$, 20Hz Update Rate
Common Mode 50/60Hz Rejection	90 90	dB min. dB min.	50/60Hz $\pm 1Hz$, Range = $\pm 20mV$ 50/60Hz $\pm 1Hz$, Range = $\pm 2.5V$
Differential Input Voltage Ranges			
$\pm REFIN/GAIN$		V nom.	REFIN refers to both REFIN1 and REFIN2. REFIN=REFIN(+)-REFIN(-) GAIN=1to 128.
Pseudo-Differential Input Voltage Ranges			
0V to REFIN/GAIN		V nom.	
Full-scale Range Matching	5	μV typ.	
Absolute Ain Voltage Limits			
Buffered Inputs	GND+50mV $V_{DD}-50mV$	V min. V max	
Unbuffered Inputs	GND-30mV $V_{DD}+30mV$	Vmin Vmax	

PARAMETER	B Grade	Units	Test Conditions
LOGIC INPUTS			
All Inputs Except SCLK and XTAL1			
V _{INL} , Input Low Voltage	0.8	V max.	V _{DD} = 5V
V _{INL} , Input Low Voltage	0.4	V max.	V _{DD} = 3V
V _{INH} , Input High Voltage	2.0	V min.	V _{DD} = 3V or 5V
SCLK Only (Schmitt Triggered Input)			
V _{T(+)}	1.4/3	V min/V max	V _{DD} = 5V
V _{T(-)}	0.8/1.4	V min/V max	V _{DD} = 5V
V _{T(+)} -V _{T(-)}	0.4/0.85	V min/V max	V _{DD} = 5V
V _{T(+)}	0.95/2.5	V min/V max	V _{DD} = 3V
V _{T(-)}	0.4/1.1	V min/V max	V _{DD} = 3V
V _{T(+)} -V _{T(-)}	0.4/0.85	V min/V max	V _{DD} = 3V
XTAL1 Only			
V _{INL} , Input Low Voltage	0.8	V max.	V _{DD} = 5V
V _{INH} , Input High Voltage	3.5	V min.	V _{DD} = 5V
V _{INL} , Input Low Voltage	0.4	V max.	V _{DD} = 3V
V _{INH} , Input High Voltage	2.5	V min.	V _{DD} = 3V
Input Currents	±10	µA max.	V _{IN} = 0V or V _{DD}
Input Capacitance	10	pF typ.	All Digital Inputs
LOGIC OUTPUTS (Excluding XTAL2)			
V _{OH} , Output High Voltage	V _{DD} - 0.6	V min.	V _{DD} = 3V, I _{SOURCE} = 100µA
V _{OL} , Output Low Voltage	0.4	V max.	V _{DD} = 3V, I _{SINK} = 100µA
V _{OH} , Output High Voltage	4	V min.	V _{DD} = 5V, I _{SOURCE} = 200µA
V _{OL} , Output Low Voltage	0.4	V max.	V _{DD} = 5V, I _{SINK} = 1.6mA
Floating State Leakage Current	±10	uA max.	
Floating State Output Capacitance	±10	pF typ.	
Data Output Coding	Binary		Unipolar Mode
	Offset Binary		Bipolar Mode
EXCITATION CURRENT SOURCES			
I1 and I2 Output Current	200	µA nom.	
I3 Output Current	25	µA nom.	
Initial Tolerance at 25°C	±10	% typ.	
Drift	20	ppm/°C typ.	
Initial Current Matching at 25°C	±1	%	Matching between I1 and I2
Drift Matching	1	ppm/°C typ.	
Line Regulation (V _{DD})	TBD	nA/V max.	V _{DD} = 5V±10%
Load Regulation	TBD	nA/V max.	
Output Compliance	AV _{DD} -0.5	V max.	
Low-Side Power Switches (SW1 and SW2)			
Ron	5	Ω typ	V _{DD} = 5V
	7	Ω typ	V _{DD} = 3V
Allowable Current	20	mA max	Per Switch
SYSTEM CALIBRATION			
Full-Scale Calibration Limit	1.05 X FS	V max.	
Zero-Scale Calibration Limit	-1.05 X FS	V min.	
Input Span	0.8 X FS	V min.	
	2.1 X FS	V max.	
START UP TIME			
From Power-On	500	msec typ.	
From Idle Mode	1	msec. typ.	
From Power-Down Mode	1	msec. typ.	
	500	msec. typ.	Osc. powered down
POWER REQUIREMENTS			
Power Supply Voltages			
V _{DD} - GND	2.7/3.6	V min/max	V _{DD} = 3V nom.
	4.5/5.5	V min/max	V _{DD} = 5V nom.

PRELIMINARY TECHNICAL DATA

AD7709

PARAMETER	B Grade	Units	Test Conditions
Power Supply Currents			
V _{DD} Current (Normal Mode)	TBD	mA	V _{DD} =3V
V _{DD} Current (Normal Mode)	TBD	mA	V _{DD} =5V
V _{DD} Current (Idle Mode)	TBD	mA	V _{DD} =3V
V _{DD} Current (Idle Mode)	TBD	mA	V _{DD} =5V
V _{DD} Current (Power-Down Mode)	20	μA max.	V _{DD} =3V, 32.768kHz Osc. Running
V _{DD} Current (Power-Down Mode)	30	μA max.	V _{DD} =5V, 32.768kHz Osc. Running

NOTES

¹ Temperature Range -40°C to +85°C

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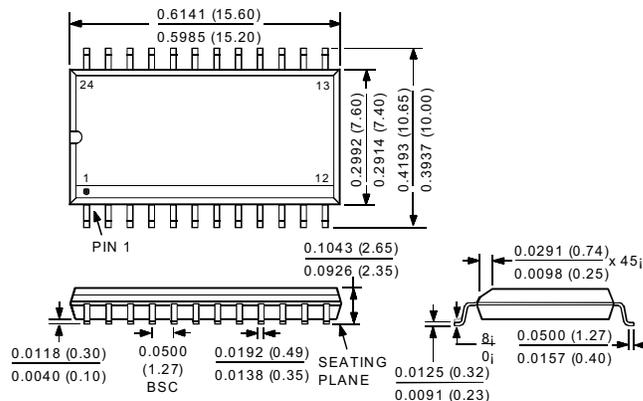
ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

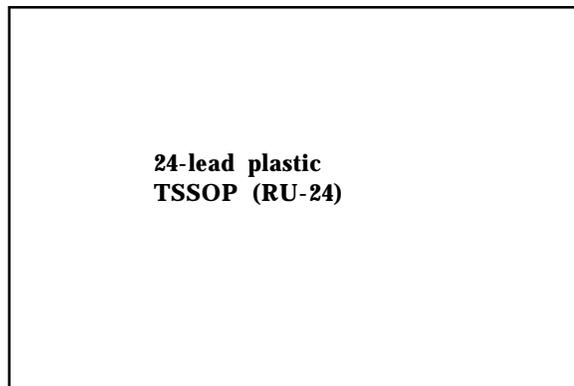
V _{DD} to GND.....	-0.3V to +7V
Analog Input Voltage to GND.....	-0.3V to V _{DD} +0.3V
Reference Input Voltage to GND.....	-0.3V to V _{DD} +0.3V
AIN/REFIN Current (Indefinite).....	30mA
Digital Input Voltage to GND.....	-0.3V to V _{DD} +0.3V
Digital Output Voltage to GND.....	-0.3V to V _{DD} +0.3V
PWRGND to GND.....	-0.3V to +0.3V
Operating Temperature Range.....	-40°C to 85°C
Storage Temperature Range.....	-65°C to 150°C
Junction Temperature.....	+150°C
PACKAGE Power Dissipation.....	TBD mW
θ _{JA} Thermal Impedance.....	90°C/W
Lead Temperature, Soldering	
Vapor Phase (60sec).....	+215°C
Infrared (15 sec).....	+220°C

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OUTLINE DIMENSIONS
24-lead plastic SOIC (R-24)



24-lead plastic TSSOP (RU-24)



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7709 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model	Temperature Range	Package Description	Package Drawing Option
AD7709BR	-40°C to +85°C	SOIC	R-24
AD7709BRU	-40°C to +85°C	TSSOP	RU-24

AD7709

TIMING CHARACTERISTICS^{1,2} ($V_{DD} = +3V \pm 10\%$ or $V_{DD} = +5V \pm 10\%$; $GND = 0V$; $X_{TAL} = 32.768kHz$; Input Logic 0 = 0V, Logic 1 = V_{DD})

unless otherwise noted)

Parameter	Limit at T_{MIN} , T_{MAX} (B Version)	Units	Conditions/Comments
t_1	32.768	kHz typ	Crystal Oscillator Frequency.
t_2	50	ns min	\overline{RESET} Pulse Width
Read Operation			
t_3	0	ns min	\overline{RDY} to \overline{CS} Setup Time
t_4	0	ns min	\overline{CS} Falling Edge to SCLK Active Edge Setup Time ³
t_5^4	0	ns min	SCLK Active Edge to Data Valid Delay ³
	60	ns max	$V_{DD} = +4.5 V$ to $+5.5 V$
	80	ns max	$V_{DD} = +2.7 V$ to $+3.6 V$
$t_{5A}^{4,5}$	0	ns min	\overline{CS} Falling Edge to Data Valid Delay ³
	60	ns max	$V_{DD} = +4.5 V$ to $+5.5 V$
	80	ns max	$V_{DD} = +2.7 V$ to $+3.6 V$
t_6	100	ns min	SCLK High Pulse Width
t_7	100	ns min	SCLK Low Pulse Width
t_8	0	ns min	\overline{CS} Rising Edge to SCLK Inactive Edge Hold Time ³
t_9^6	10	ns min	Bus Relinquish Time after SCLK Inactive Edge ³
	80	ns max	
t_{10}	100	ns max	SCLK Active Edge to \overline{RDY} High ^{3, 7}
Write Operation			
t_{11}	0	ns min	\overline{CS} Falling Edge to SCLK Active Edge Setup Time ³
t_{12}	30	ns min	Data Valid to SCLK Edge Setup Time
t_{13}	25	ns min	Data Valid to SCLK Edge Hold Time
t_{14}	100	ns min	SCLK High Pulse Width
t_{15}	100	ns min	SCLK Low Pulse Width
t_{16}	0	ns min	\overline{CS} Rising Edge to SCLK Edge Hold Time

NOTES

¹ Sample tested during initial release to ensure compliance. All input signals are specified with $t_r = t_f = 5 ns$ (10% to 90% of V_{DD}) and timed from a voltage level of 1.6V.

² See Figures 1 and 2.

³ SCLK active edge is falling edge of SCLK.

⁴ These numbers are measured with the load circuit of Figure 3 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

⁵ This specification only comes into play if \overline{CS} goes low while SCLK is low. It is required primarily for interfacing to DSP machines.

⁶ These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 3. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

⁷ \overline{RDY} returns high after the first read from the device after an output update. The same data can be read again, if required, while \overline{RDY} is high, although care should be taken that subsequent reads do not occur close to the next output update.

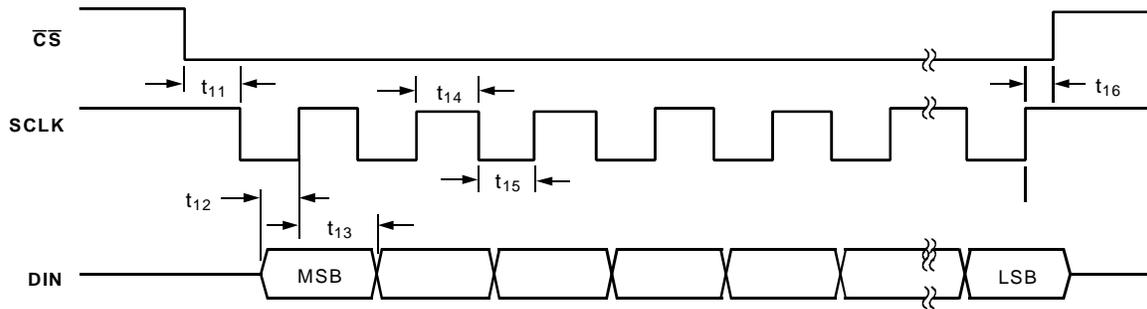


Figure 1. Write Cycle Timing Diagram

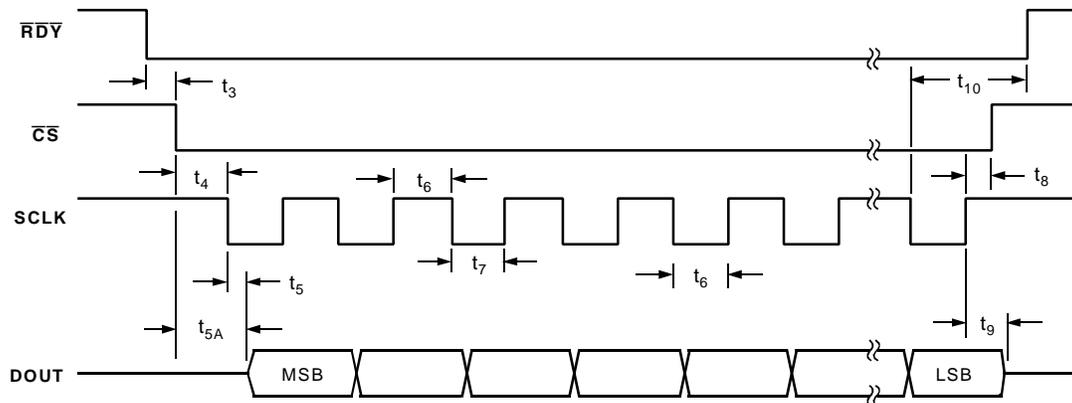
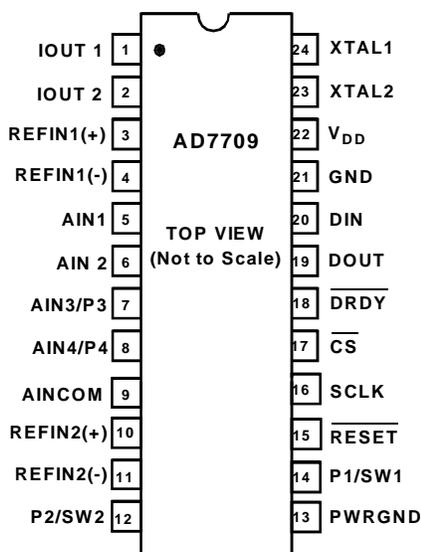


Figure 2. Read Cycle Timing Diagram

AD7709

PIN CONFIGURATION



Pin Function Description

Pin No	Mnemonic	Function
1	IOUT1	Output for internal excitation current sources. A single current source or any combination of the internal current sources I1,I2 and I3 can be switched to this output.
2	IOUT2	Output for internal excitation current sources. A single current source or any combination of the internal current sources I1,I2 and I3 can be switched to this output.
3	REFIN1(+)	Positive reference input. REFIN(+) can lie anywhere between V_{DD} and GND. The nominal reference voltage (REFIN(+)-REFIN(-)) is 2.5V but the part is functional with a reference range from 1V to V_{DD} .
4	REFIN1(-)	Negative reference input. This reference input can lie anywhere between GND and V_{DD} -1V.
5	AIN1	Analog Input Channel 1. Programmable-gain analog input which can be used as a pseudo-differential input when used with AINCOM or as the positive input of a fully-differential input pair when used with AIN2. (see Communications Register section)
6	AIN2	Analog Input Channel 2. Programmable-gain analog input which can be used as a pseudo-differential input when used with AINCOM or as the negative input of a fully-differential input pair when used with AIN1. (see Communications Register section)
7	AIN3/P3	Analog Input Channel 3 or Digital Port Bit. Programmable-gain analog input which can be used as a pseudo-differential input when used with AINCOM or as the positive input of a fully-differential input pair when used with AIN4. The second function of this bit is as a general purpose digital input bit.
8	AIN4/P4	Analog Input Channel 4 or digital port bit. Programmable-gain analog input which can be used as a pseudo-differential input when used with AINCOM or as the negative input of a fully-differential input pair when used with AIN3. The second function of this bit is as a general purpose digital input bit.
9	AINCOM	All analog inputs are referenced to this input when configured in pseudo-differential input mode.
10	REFIN2(+)	Positive reference input. REFIN2(+) can lie anywhere between V_{DD} and GND. The nominal reference voltage (REFIN2(+)-REFIN2(-)) is 2.5V but the part is functional with a reference range from 1V to V_{DD} .

11	REFIN2(-)	Negative reference input. This reference input can lie anywhere between GND and $V_{DD}-1V$.
12	P2/SW2	P2 can act as a general purpose Input/Output bit referenced between V_{DD} and GND or as a low-side power switch to PWRGND..
13	PWRGND	Ground point for the low-side power switches SW2 and SW1. PWRGND must be tied to GND.
14	P1/SW1	P1 can act as a general purpose Output bit referenced between V_{DD} and GND or as a low-side power switch to PWRGND.
15	$\overline{R\overline{E}S\overline{E}T}$	Digital input used to reset the ADC to its power-on-reset status. This pin has a weak pull-up internally to DV_{DD} .
16	SCLK	Serial clock input for data transfers to and from the ADC. The SCLK has a schmitt triggered input making the interface suitable for opto-isolated applications. The serial clock can be continuous with all data transmitted in a continuous train of pulses. Alternatively, it can be noncontinuous clock with the information being transmitted to or from the AD7709 in smaller batches of data.
17	\overline{CS}	Chip Select Input. This is an active low logic input used to select the AD7709. \overline{CS} can be used to select the AD7709 in systems with more than one device on the serial bus or as a frame synchronisation signal in communicating with the device. \overline{CS} can be hardwired low allowing the AD7709 to be operated in three-wire mode with SCLK, DIN and DOUT used to interface with the device.
18	\overline{RDY}	\overline{RDY} is a logic low status output from the AD7709. \overline{RDY} is low if the ADC has valid data in its data register. This output returns high on completion of a read operation from the data register. If data is not read, \overline{RDY} will return high prior to the next update indicating to the user that a read operation should not be initiated.
19	DOUT	Serial data output with serial data being read from the output shift register of the ADC. The output shift register can contain data from any of the on-chip data, calibration or control registers.
20	DIN	Serial Data Input with serial data being written to the input shift register on the AD7709. Data in this shift register is transferred to the control registers within the ADC depending on the selection bits of the Communications register.
21	GND	Ground Reference point for the AD7709.
22	V_{DD}	Supply voltage, 3V or 5V nominal.
23	XTAL2	Output from the 32kHz crystal oscillator inverter.
24	XTAL1	Input to the 32kHz crystal oscillator inverter.

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ADC CIRCUIT INFORMATION

Overview

The AD7709 incorporates an analog multiplexer with a Sigma-Delta ADC, on-chip programmable gain amplifier and digital filtering intended for the measurement of wide dynamic range, low frequency signals such as those in weigh-scale, strain-gauge, pressure transducer or temperature measurement applications. The AD7709 offers 16-bit resolution. The AD7709 can be configured as 2 fully differential input channels or as 4 pseudo differential input channels referenced to AINCOM. The channel is buffered and can be programmed for one of 8 input ranges from $\pm 20\text{mV}$ to $\pm 2.56\text{V}$. Buffering the input channel means that the part can handle significant source impedances on the analog input and that R, C filtering (for noise rejection or RFI reduction) can be placed on the analog inputs if required. These input channels are intended to convert signals directly from sensors without the need for external signal conditioning. Other functions contained on-chip that augment the operation of the ADC include software configurable current sources, switchable reference inputs and low side power switches.

The ADC employs a sigma-delta conversion technique to realize up to 16-bits of no missing codes performance. The sigma-delta modulator converts the sampled input signal into a digital pulse train whose duty cycle contains the digital information. A Sinc^3 programmable low pass filter is then employed to decimate the modulator output data stream to give a valid data conversion result at programmable output rates from 5.35Hz (186.77mS) to 105.03Hz (9.52mS). A Chopping scheme is also employed to minimize ADC channel offset errors. A block diagram of the ADC input channel is shown in Figure 3 below.

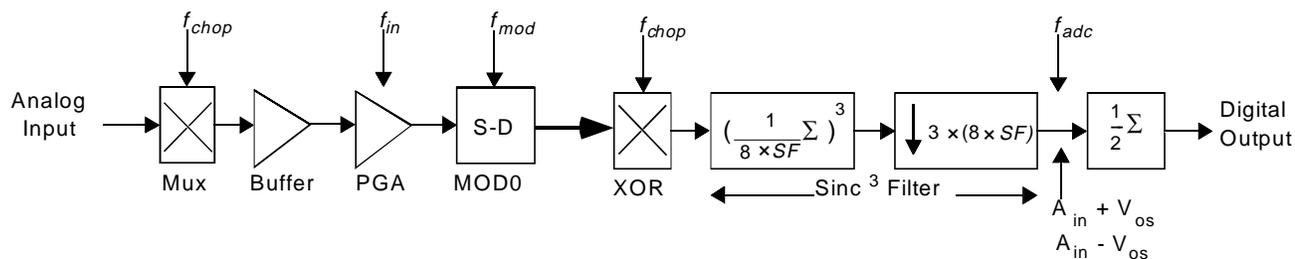


Figure 3. AD7709 ADC Channel Block Diagram

ADC NOISE PERFORMANCE

Tables I and II below show the output rms noise and output peak-to-peak resolution in bits (rounded to the nearest 0.5LSB) for some typical output update rates . The numbers are typical and generated at a differential input voltage of 0V. The output update rate is selected via the SF7-SF0 bits in the Filter Register. It is important to note that the peak-to-peak resolution figures represent the resolution for which there will be no code flicker within a six-sigma limit. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independant of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in the tables are given for the bipolar input ranges. For the unipolar ranges the rms noise numbers will be the same as the bipolar range but the peak to peak resolution is now based on half the signal range which effectively means loosing 1 bit of resolution.

Table I. Typical Output RMS Noise vs. Input Range and Update Rate for AD7709
Output RMS Noise in μV

SF Word	Data Update Rate (Hz)	Input Range							
		$\pm 20\text{mV}$	$\pm 40\text{mV}$	$\pm 80\text{mV}$	$\pm 160\text{mV}$	$\pm 320\text{mV}$	$\pm 640\text{mV}$	$\pm 1.24\text{V}$	$\pm 2.56\text{V}$
13	105.3	1.50	1.50	1.60	1.75	3.50	4.50	6.70	11.75
69	19.79	0.60	0.65	0.65	0.65	0.65	0.95	1.40	2.30
255	5.35	0.35	0.35	0.37	0.37	0.37	0.51	0.82	1.25

Table II. Peak-to-Peak Resolution vs. Input Range and Update Rate for AD7709
Peak-to-Peak Resolution in Bits

SF Word	Data Update Rate (Hz)	Input Range							
		$\pm 20\text{mV}$	$\pm 40\text{mV}$	$\pm 80\text{mV}$	$\pm 160\text{mV}$	$\pm 320\text{mV}$	$\pm 640\text{mV}$	$\pm 1.24\text{V}$	$\pm 2.56\text{V}$
13	105.3	12	13	14	15	15	15.5	16	16
69	19.79	13	14	15	16	16	16	16	16
255	5.35	14	15	16	16	16	16	16	16

AD7709 ON-CHIP REGISTERS

Both the AD7709 is controlled and configured via 4 on-chip registers as shown in figure 4 and described in more detail in the following section. In the following descriptions, **SET** implies a logic 1 state and **CLEARED** implies a logic 0 state unless otherwise stated.

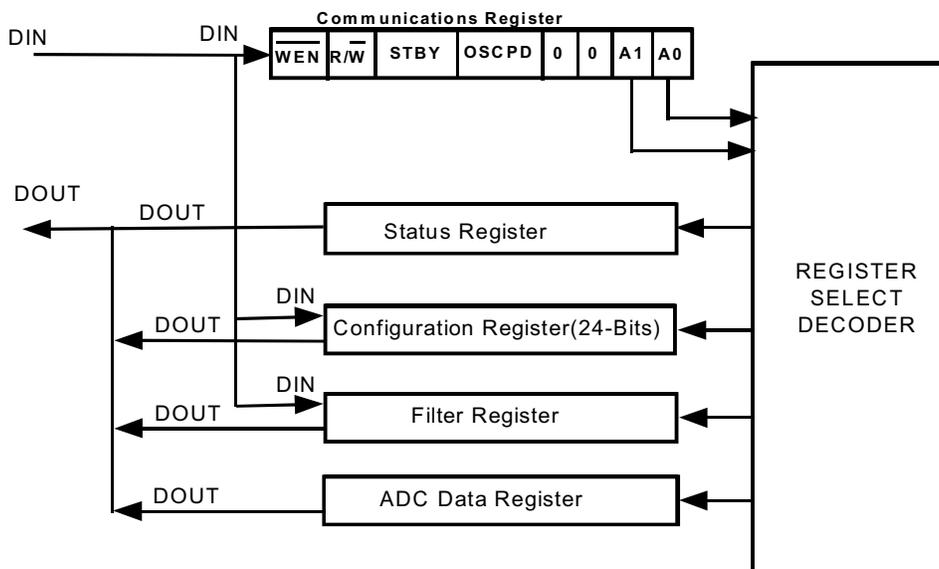


Figure 4. AD7709 On-Chip Registers

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Communications Register- (A1, A0= 0,0):

The Communications Register is an 8-bit write-only register. All communications to the part must start with a write operation to the Communications Register. The data written to the Communications Register determines whether the next operation is a read or write operation, the type of read operation and to which register this operation takes place. For read or write operations, once the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the Communications Register. This is the default state of the interface, and on power-up or after a RESET, the AD7709 is in this default state waiting for a write operation to the Communications Register. In situations where the interface sequence is lost, a write operation of at least 32 serial clock cycles with DIN high, returns the AD7709 to this default state by resetting the part. Table III outlines the bit designations for the Communications Register. CR0 through CR7 indicate the bit location, CR denoting the bits are in the Communications Register. CR7 denotes the first bit of the data stream.

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
$\overline{\text{WEN}}(0)$	$\text{R}/\overline{\text{W}}(0)$	$\text{STBY}(0)$	$\text{OSCPD}(0)$	$0(0)$	$0(0)$	$\text{A1}(0)$	$\text{A}(0)$

Table III. Communications Register Bit Designations

Bit Location	Bit Mnemonic	Description
CR7	$\overline{\text{WEN}}$	Write Enable Bit. A 0 must be written to this bit so the write operation to the Communications Register actually takes place. If a 1 is written to this bit, the part will not clock on to subsequent bits in the register. It will stay at this bit location until a 0 is written to this bit. Once a 0 is written to the $\overline{\text{WEN}}$ bit, the next seven bits will be loaded to the Communications Register.
CR6	$\text{R}/\overline{\text{W}}$	A zero in this bit location indicates that the next operation will be a write to a specified register. A one in this position indicates that the next operation will be a read from the designated register.
CR5	STBY	Standby bit indication. Set when its required to put the AD7709 in low power mode. Clear to power up the AD7709.
CR4	OSCPD	Oscillator Power Down Bit. If this bit is set , then placing the AD7709 in standby mode will stop the crystal oscillator reducing the power drawn by these parts to a minimum. The oscillator will require 500ms to begin oscillating when the ADC is taken out of standby mode. If this bit is cleared the oscillator is not shut off when the ADC is put into standby mode and will not require the 500ms start-up time when the ADC is taken out of standby.
CR3	0	This bit must be programmed with a logic 0 for correct operation.
CR2	0	This bit must be programmed with a logic 0 for correct operation.
CR1-CR0	A1-A0	Register Address Bits. These address bits are used to address the AD7709's registers and are outlined in table IV.

Table IV. AD7709 Register Selection Table

A1	A0	Register
0	0	Communications register during a write operation.
0	0	Status Register register during a read operation.
0	1	Configuration Register
1	0	Filter register
1	1	ADC Data Register

Status Register - (A1,A0=0,0; Power-On-Reset = 00Hex):

The ADC Status Register is an 8-bit read-only register. To access the ADC Status Register, the user must write to the Communications Register selecting the next operation to be a read and load bits A1-A0 with 0,0. Table V outlines the bit designations for the Status Register. SR0 through SR7 indicate the bit location, SR denoting the bits are in the Status Register. SR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit.

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
RDY(0)	0(0)	0(0)	0(0)	ERR (0)	0(0)	STBY(0)	LOCK(0)

Table V. Status Register Bit Designations

Bit Location	Bit Mnemonic	Description
SR7	RDY	Ready bit for the ADC Set when data is transferred to the ADC data register. The RDY bit is cleared automatically a period of time before the data register is updated with a new conversion result or after the ADC data register has been read.
SR6	0	Bit is automatically cleared . Reserved for future use
SR5	0	This bit is automatically cleared . Reserved for future use
SR4	0	This bit is automatically cleared . Reserved for future use
SR3	ERR	ADC Error Bit. This qualifying bit is set at the same at the RDY bit. When Set it indicates that the result written to the ADC data register has been clamped to all zeros or all ones. Error sources include Overrange and loss of lock. This bit is Cleared at the same time as the RDY bit.
SR2	0	This bit is automatically cleared . Reserved for future use
SR1	STBY	Standby bit indication. When Set it indicates that the AD7709 is in low power mode. Cleared when the ADC is powered up.
SR0	LOCK	PLL lock status bit. This bit is SET if the PLL has locked onto the 32kHz crystal oscillator clock. The ADC will not start conversion till this bit has been set. If the LOCK bit subsequently goes low the ERR bit will be set.

Configuration Register(CONFIG) :(A1,A0 = 0,1; Power-On-Reset = 00000Hex)

The CONFIG Register is a 24-bit register from which data can either be read or to which data can be written. This register is used to select the input channel and configure the input range, excitation current sources and I/O port. Table XIII outlines the bit designations for this register. CONFIG24 through CONFIG0 indicate the bit location, CONFIG denoting the bits are in the Configuration Register. CONFIG24 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. A write to the CONFIG register has immediate effect and does not reset the the ADCs. Thus , if a current source is switched while the ADC is converting the user will have to wait for the fullsettling time of the sinc³ filter before getting a fully settled output. This equates to 4 outputs.

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CONFIG23	CONFIG22	CONFIG21	CONFIG20	CONFIG19	CONFIG18	CONFIG17	CONFIG16
PSW1(0)	PSW2(0)	I3EN1 (0)	I3EN1(0)	I2EN1(0)	I2EN0(0)	I1EN1(0)	I1EN0(0)
CONFIG15	CONFIG14	CONFIG13	CONFIG12	CONFIG11	CONFIG10	CONFIG9	CONFIG8
P4DIG(0)	P3DIG(0)	P2EN(0)	P1EN(0)	P4DAT(0)	P3DAT(0)	P2DAT(0)	P1DAT(0)
CONFIG7	CONFIG6	CONFIG5	CONFIG4	CONFIG3	CONFIG2	CONFIG1	CONFIG0
REFSEL(0)	CH2(0)	CH1(0)	CH0(0)	UNI(0)	RN2(0)	RN1(0)	RN0(0)

Table VI. Configuration Register Bit Designations

Bit	Bit	Description															
Location	Mnemonic	Description															
CONFIG23	PSW1	Power Switch 1 Control bit. Set by user to enable Power switch P1 to PWRGND. Cleared by user to enable use as a standard I/O pin. When ADC is in standby mode the power switches are open.															
CONFIG22	PSW2	Power Switch 2 Control bit. Set by user to enable Power switch P2 to PWRGND. Cleared by user to enable use as a standard I/O pin. When ADC is in standby mode the power switches are open.															
CONFIG21	I3EN1	Current Source Enable Bits. Used in conjunction with bit I3EN0 to determine the function of current source I3															
CONFIG20	I3EN0	Current Source Enable Bits. Used in conjunction with bit I3EN1 to determine the function of current source I3 <table border="1"> <thead> <tr> <th>I3EN1</th> <th>I3EN0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Current Source OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>Current Source Routed to IOUT1 pin.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Current Source Routed to IOUT2 pin.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Current Source Routed to GND</td> </tr> </tbody> </table>	I3EN1	I3EN0	Function	0	0	Current Source OFF	0	1	Current Source Routed to IOUT1 pin.	1	0	Current Source Routed to IOUT2 pin.	1	1	Current Source Routed to GND
I3EN1	I3EN0	Function															
0	0	Current Source OFF															
0	1	Current Source Routed to IOUT1 pin.															
1	0	Current Source Routed to IOUT2 pin.															
1	1	Current Source Routed to GND															
CONFIG19	I2EN1	Current Source Enable Bits. Used in conjunction with bit I2EN0 to determine the function of current source I2															
CONFIG18	I2EN0	Current Source Enable Bits. Used in conjunction with bit I2EN1 to determine the function of current source I2 <table border="1"> <thead> <tr> <th>I2EN1</th> <th>I2EN0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Current Source OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>Current Source Routed to IOUT1 pin.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Current Source Routed to IOUT2 pin.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Current Source Routed to GND</td> </tr> </tbody> </table>	I2EN1	I2EN0	Function	0	0	Current Source OFF	0	1	Current Source Routed to IOUT1 pin.	1	0	Current Source Routed to IOUT2 pin.	1	1	Current Source Routed to GND
I2EN1	I2EN0	Function															
0	0	Current Source OFF															
0	1	Current Source Routed to IOUT1 pin.															
1	0	Current Source Routed to IOUT2 pin.															
1	1	Current Source Routed to GND															
CONFIG17	I1EN1	Current Source Enable Bits. Used in conjunction with bit I1EN0 to determine the function of current source I3															
CONFIG16	I1EN0	Current Source Enable Bits. Used in conjunction with bit I1EN1 to determine the function of current source I3 <table border="1"> <thead> <tr> <th>I1EN1</th> <th>I1EN0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Current Source OFF</td> </tr> <tr> <td>0</td> <td>1</td> <td>Current Source Routed to IOUT1 pin.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Current Source Routed to IOUT2 pin.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Current Source Routed to GND</td> </tr> </tbody> </table>	I1EN1	I1EN0	Function	0	0	Current Source OFF	0	1	Current Source Routed to IOUT1 pin.	1	0	Current Source Routed to IOUT2 pin.	1	1	Current Source Routed to GND
I1EN1	I1EN0	Function															
0	0	Current Source OFF															
0	1	Current Source Routed to IOUT1 pin.															
1	0	Current Source Routed to IOUT2 pin.															
1	1	Current Source Routed to GND															
CONFIG15	P4DIG	Digital Input Enable Set by user to enable P4 as a digital input Cleared by user to configure as pin P4/AIN4 as analog input.															

CONFIG14	P3DIG	Digital Input Enable Set by user to enable P3 as a digital input Cleared by user to configure as pin P3/AIN3 as analog input. The default configuration is analog input.
CONFIG13	P2EN	P2 digital output enable bit. Set by user to enable P2 as a regular digital output pin. Cleared by user to tristate P2 output. PSW2 takes presedance over P2EN.
CONFIG12	P1EN	P1 digital output enable bit. Set by user to enable P1 as a regular digital output pin. Cleared by user to tristate P1 output. PSW1 takes presedance over P1EN.
CONFIG11	P4DAT	Digital input port data bit. P4DAT is read only and will return a 0 if P4DIG=0. If P4 is enabled as a digital input then the read back value indicates the status of pin P4.
CONFIG10	P3DAT	Digital input port data bit. P3DAT is read only and will return a 0 if P3DIG=0. If P3 is enabled as a digital input then the read back value indicates the status of pin P3.
CONFIG9	P2DAT	Digital output port data bit. P2 is digital output only. When the port is active as an output (P2EN=1), then the value written to the this data bit appears at the output port. Reading P2DAT will return what was last written to the P2DAT bit on the AD7709.
CONFIG8	P1DAT	Digital output port data bit. P1 is digital output only. When the port is active as an output (P1EN=1), then the value written to the this data bit appears at the output port. Reading P1DAT will return what was last written to the P1DAT bit on the AD7709.
CONFIG7	REFSEL	ADC reference input select. Cleared by user to select REFIN1(+) and REFIN1(-) as the ADC reference. Set by user to select REFIN2(+) and REFIN2(-) as the ADC reference.
CONFIG6	CH2	ADC Input Channel Selection bit. Used in conjunction with CH1 and CH0 as shown in the analog input selection table.
CONFIG5	CH1	ADC Input Channel Selection bit. Used in conjunction with CH2 and CH0 as shown in the analog input selection table.
CONFIG4	CH0	ADC Input Channel Selection bit. Used in conjunction with CH2 and CH2 as shown in the analog input selection table.

CH2	CH1	CH0	Positive Input	Negative Input	Buffer
0	0	0	AIN1	AINCOM	Positive Analog Input
0	0	1	AIN2	AINCOM	Positive Analog Input
0	1	0	AIN3	AINCOM	Positive Analog Input
0	1	1	AIN4	AINCOM	Positive Analog Input
1	0	0	AIN1	AIN2	Positive and Negative Analog Inputs
1	0	1	AIN3	AIN4	Positive and Negative Analog Inputs
1	1	0	AINCOM	AINCOM	Positive and Negative Analog Inputs

The final column indicates if the analog inputs are buffered or unbuffered. This determines the common mode input range on each input. If the input is unbuffered (AINCOM) the common mode input includes GND.

CONFIG3	UNI	Unipolar/Bipolar Operation Selection Bit. Set by user to enable unipolar operation with straight binary output coding i.e. zero differential input will result in 0000hex output and a fullscale differential input will result in FFFF Hex output. Cleared by user to enable pseudo bipolar operation and offset binary coding, negative fullscale differential input will result in an output code of 0000 Hex, zero differential input will result in an output code of 8000Hex and a positive fullscale differential input will result in an output code of FFFF Hex.
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AD7709

CONFIG2	RN2	Used in conjunction with RN1 and RN0 to select the analog input range.		
CONFIG1	RN1	Used in conjunction with RN2 and RN0 to select the analog input range.		
CONFIG0	RN0	Used in conjunction with RN2 and RN1 to select the analog input range.		
	RN2	RN1	RN0	Selected Main ADC Input Range (Vref=2.5V)
	0	0	0	±20mV
	0	0	1	±40mV
	0	1	0	±80mV
	0	1	1	±160mV
	1	0	0	±320mV
	1	0	1	±640mV
	1	1	0	±1.28V
	1	1	1	±2.56V

Filter Register: (A1,A0=1,0; Power-On-Reset = 00Hex)

The Filter Register is an 8-bit register from which data can either be read or to which data can be written. This register determines the amount of averaging performed by the sinc filter. Table VII outlines the bit designations for the Filter Register. FR7 through FR0 indicate the bit location, FR denoting the bits are in the Filter Register. FR7 denotes the first bit of the data stream. The number in brackets indicates the power-on/reset default status of that bit. The number in this register is used to set the decimation factor and thus the output update rate for the ADCs. The filter register cannot be written to by the user while the ADC is active. The update rate is used for the ADC is calculated as follows :

$$f_{adc} = \frac{1}{3} \times \frac{1}{8.SF} \times f_{mod}$$

Where :
 f_{adc} = ADC Output Update Rate
 f_{mod} = Modulator Clock Frequency= 32.768KHz (Main and Aux ADC)
 SF = Decimal Value written to SF Register

FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
SF7(0)	SF6(1)	SF5(0)	SF4(0)	SF3(0)	SF2(1)	SF1(0)	SF0(1)

Table VII. Filter Register Bit Designations

The allowable range for SF is 13dec to 255dec. Examples of SF values and corresponding conversion rate (f_{adc}) and time (t_{adc}) are shown in table XII below. It should also be noted that both ADC input channels are chopped to minimise offset errors. This means that the time for a single conversion or the time to the first conversion result is 2 X t_{adc}.

SF(dec)	SF(hex)	f _{adc} (Hz)	t _{adc} (ms)
13	0D	105.3	9.52
69	45	19.79	50.34
255	FF	5.35	186.77

Table XII. Update Rate Vs SF Word.

ADC Data Result Register (DATA):(A1,A0=1,1; Power-On-Reset = 000000Hex)

The conversion result for the selected ADC channel is stored in the ADC data register (DATA). This register is 16-bits wide. This is a read only register. On completion of a read from this register the RDY bit in the status register is cleared.

CONFIGURING THE AD7709

On the AD7709 there are only four user accessible registers and these are configured via the serial interface. Communication with any of these registers is initiated by firstly writing to the Communications Register. The AD7709 starts converting after a power up without the requiring any register to be written to. The defaults conditions are used and the AD7709 operates at a 20Hz update rate offering 50 and 60Hz rejection.

Figure 5 outlines a flow diagram of the sequence used to configure the registers on the AD7709 following a power-up. The flowchart shows two methods of determining when its valid to read the data register. The first method is hardware polling of the RDY pin and the second method involves software interrogation of bits in the status and mode registers. The flowchart details all the necessary programming steps required to initialize the ADC and read data from the selected ADC channel following a power-on or reset. The steps can be broken down as follows:

1. Configure and initialize the microcontroller or microprocessor serial port.
2. Initialize the AD7709 by configuring the following registers:
 - a) FILTER registers which determines the update rate. The AD7709 must be put into standby mode before writing to the filter register.
 - b) CONFIGURATION register to select the input channel to be converted, its input range and reference. This register is also used to configure the internal current sources, power switches and I/O port.

Both of these operations consist of a write to the communications register to specify the next operation as a write to a specified register. Data is then written to this register. When each sequence is complete the ADC defaults to waiting for another write to the communications register to specify the next operation.

3) When configuration is complete the user needs to determine when its valid to read the data from the data register. This is accomplished by either polling the RDY pin (hardware polling) or by interrogating the bits in the STATUS register (software polling). Both are shown in the following flowchart.

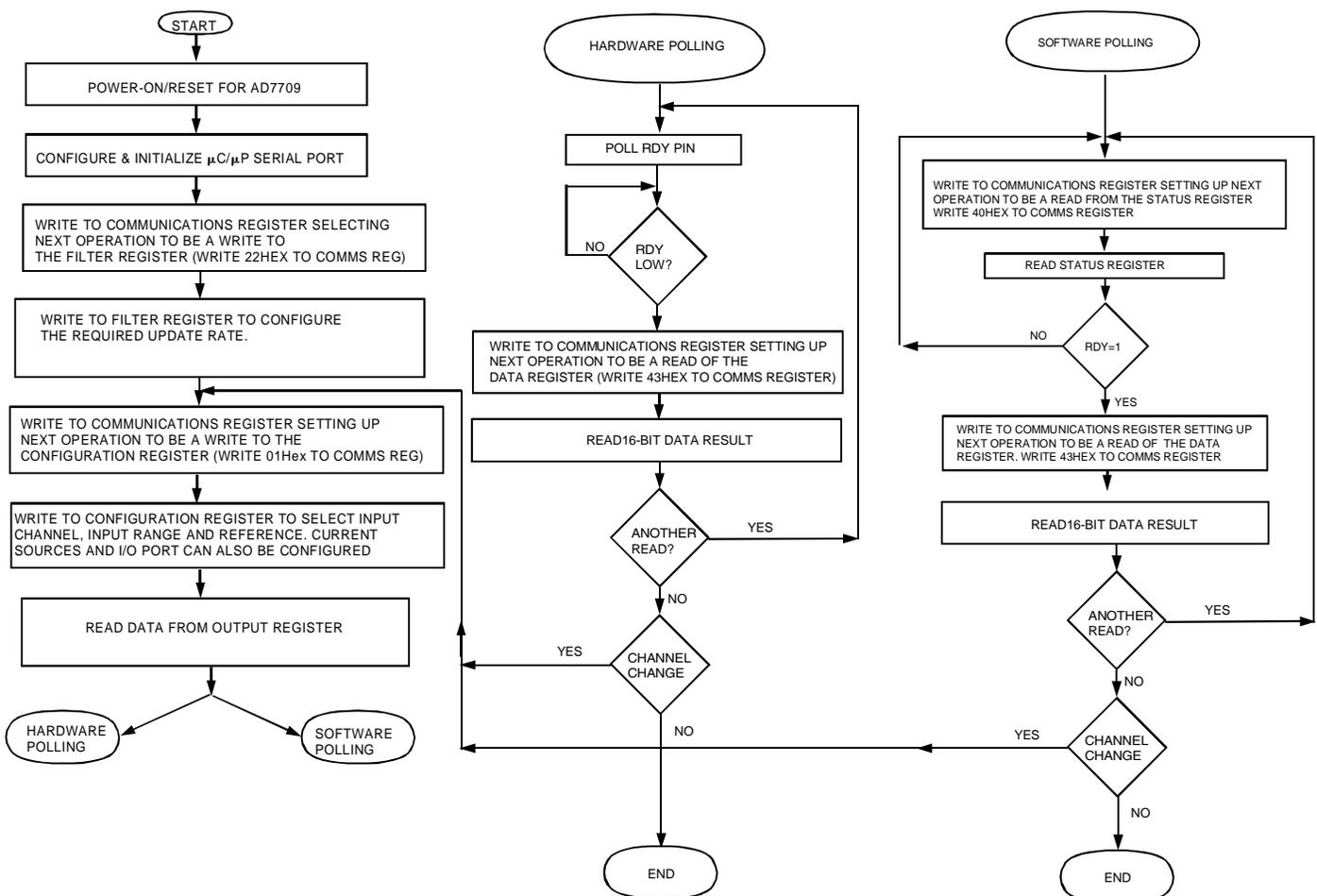


Figure 5. Flowchart for Configuring and reading from AD7709