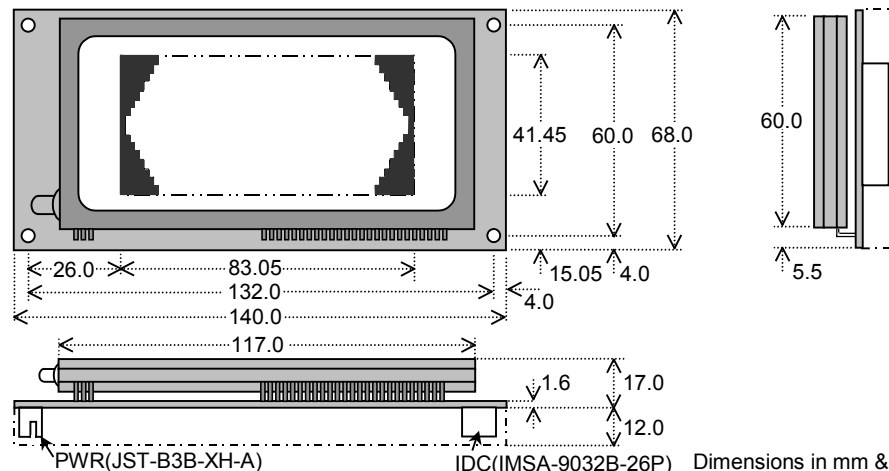


Dot Graphic VFD Module

GU128X64-800

- ❑ 128 x 64 Dot Graphic
- ❑ Operating Temp -40°C to +85°C
- ❑ Single 5V Supply.
- ❑ High Brightness Blue Green Display
- ❑ Selectable Parallel (i80/M68)/Serial Interface
- ❑ Twin Screen Graphic RAM
- ❑ 16 Level Brightness Control Function

The module includes the Vacuum Fluorescent Display glass, driver and control ASIC, with integral refresh Graphic RAM and logic for parallel and synchronous serial interfaces. The high speed 8 bit parallel interface is 5V CMOS compatible suitable for connection to a host CPU bus. Brightness control and power down functions are provided. A full data sheet is available.



Dimensions in mm & subject to tolerances.
Mounting holes 3.5mm dia.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Condition
Power Supply Voltage	Vcc	5.0VDC +/- 5%	GND=0V
Power Supply Current	Icc	750mADC typ.	Vcc= 5V
Logic High Input	V _{IH}	0.8Vcc VDC min.	I _{IH} = 2uA
Logic Low Input	V _{IL}	0.2Vcc VDC max.	I _{IL} = -600uA
Logic High Output	V _{OH}	Vcc-0.3VDC min.	I _{OH} = -300uA
Logic Low Output	V _{OL}	0.3 VDCmax.	I _{OL} = 300uA

The power on rise time should be less than 100ms. The inrush current at power on can be 2 x Icc.

OPTICAL AND ENVIRONMENTAL SPECIFICATIONS

Parameter	Value
Display Area (XxY mm)	83.05 x 41.45
Dot Size/Pitch (XxY mm)	0.5 x 0.5/0.65 x 0.65
Luminance	350 cd/m ² Min.
Colour of Illumination	Blue-Green (Filter for colours)
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +85°C
Operating Humidity (non condensing)	20 to 80% RH @ 25°C

SOFTWARE COMMANDS

Instruction	C/D	Command Byte	No. Bytes
Set Display On/Off / Layer Merge	1	20H→2FH	2
Set Display Brightness	1	40H→4FH	1
Clear Display	1	52H→5FH	1
Set Cursor XY Address	1	60H→67H	3
Set Display Start X Address	1	70H→7FH	2
Set Write Address Mode	1	80H→8FH	1
Scroll Display Vertically Up/Down	1	B0H→BFH	1
Read Cursor XY Address	1	D4H→D7H	3
Write Data	0	00H→FFH	1

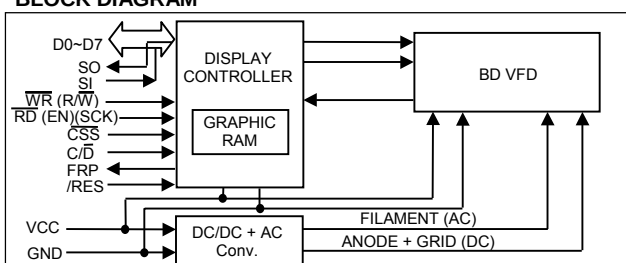
TIMING PARAMETERS (min)

i80/M68 Parameters	Time	Serial Parameters	Time
Write WR/EN Cycle Time	750ns	SCK Cycle Time	500ns
Write WR/EN Pulse Width	100ns	SCK Pulse Width	200ns
Hold after Write WR/EN	30ns	Delay After 8 th bit, CSS="L"	150ns
Set Up To Write WR/EN	30ns	Set Up To SCK, CSS="L"	60ns

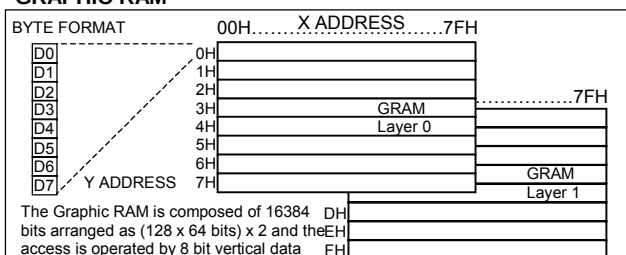
SCROLLING GRAPHIC DISPLAY

The pattern in GRAM can be scrolled around the display. Horizontal scroll is achieved by increment/decrement of the Display Start X Address. The vertical scroll process considers layer 0, then layer 1 as a continuous 128 bit high vertical area within RAM.

BLOCK DIAGRAM



GRAPHIC RAM



The Graphic RAM is composed of 16384 bits arranged as (128 x 64 bits) x 2 and the access is operated by 8 bit vertical data.

IDC DATA CONNECTOR

Pin	i80	M68	Serial	Pin	Sig
1	D7	D7	X	2	GND
3	D6	D6	X	4	GND
5	D5	D5	X	6	GND
7	D4	D4	X	8	GND
9	D3	D3	X	10	GND
11	D2	D2	X	12	GND
13	D1	D1	SO	14	GND
15	D0	D0	SI	16	GND
17	WR	R/W	X	18	GND
19	C/D	C/D	C/D	20	GND
21	RD	EN	SCK	22	GND
23	CSS	CSS	CSS	24	GND
25	FRP	FRP	FRP	26	/RES

3 PIN POWER CONNECTOR

Pin	Sig
1	Vcc
2	Test (Factory only)
3	GND

PCB JUMPERS (Open (L)ink)

Interface	J1	J2
Serial	O / L	L
i80 Parallel	O	O
M68 Parallel	L	O

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