

# SN74GTLPH1655

## 16-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE UNIVERSAL BUS TRANSCEIVER

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- Member of Texas Instruments' Widebus™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode
- TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes
- OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference
- Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels
- Partitioned as Two 8-Bit Transceivers With Individual Latch Timing and Output Control, but With a Common Clock
- LVTTL Interfaces Are 5-V Tolerant
- High-Drive GTLP Outputs (100 mA)
- LVTTL Outputs (–24 mA/24 mA)
- Variable Edge-Rate Control (ERC) Input Selects GTLP Rise and Fall Times for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads
- $I_{off}$ , Power-Up 3-State, and BIAS  $V_{CC}$  Support Live Insertion
- Bus Hold on A-Port Data Inputs
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

**DGG PACKAGE  
(TOP VIEW)**

1OEAB	1	64	CLK
1OEBA	2	63	1LEAB
$V_{CC}$	3	62	1LEBA
1A1	4	61	ERC
GND	5	60	GND
1A2	6	59	1B1
1A3	7	58	1B2
GND	8	57	GND
1A4	9	56	1B3
GND	10	55	1B4
1A5	11	54	1B5
GND	12	53	GND
1A6	13	52	1B6
1A7	14	51	1B7
$V_{CC}$	15	50	$V_{CC}$
1A8	16	49	1B8
2A1	17	48	2B1
GND	18	47	GND
2A2	19	46	2B2
2A3	20	45	2B3
GND	21	44	GND
2A4	22	43	2B4
2A5	23	42	2B5
GND	24	41	$V_{REF}$
2A6	25	40	2B6
GND	26	39	GND
2A7	27	38	2B7
$V_{CC}$	28	37	2B8
2A8	29	36	BIAS $V_{CC}$
GND	30	35	2LEAB
2OEAB	31	34	2LEBA
2OEBA	32	33	OE

### description

The SN74GTLPH1655 is a high-drive, 16-bit UBT™ transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. It is partitioned as two 8-bit transceivers and allows for transparent, latched, and clocked modes of data transfer. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to 11  $\Omega$ .



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#### description (continued)

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLP1655 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL ( $V_{TT} = 1.2\text{ V}$  and  $V_{REF} = 0.8\text{ V}$ ) or GTLP ( $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$ ) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs.  $V_{REF}$  is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using  $I_{off}$ , power-up 3-state, and BIAS  $V_{CC}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS  $V_{CC}$  circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between GND and  $V_{CC}$  adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ( $\overline{OE}$ ) input should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLP1655DGGR	GTLP1655

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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## functional description

The SN74GTLP1655 is a high-drive (100 mA), 16-bit UBT transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent, latched, or clocked modes. The device is uniquely partitioned as two 8-bit transceivers with individual latch timing and output signals and a common clock for both transceiver words. It can replace any of the functions shown in Table 1. Data polarity is noninverting.

**Table 1. SN74GTLP1655 UBT Transceiver Replacement Functions**

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541
Latched transceiver	'543			'16543
Latch	'373, '573	'843	'841	'16373
Registered transceiver	'646, '652			'16646, '16652
Flip-flop	'374, '574		'821	'16374
SN74GTLP1655 UBT transceiver replaces all above functions				

Data flow for each word is determined by the respective latch enables (xLEAB and xLEBA), output enables (xOEAB and xOEBA), and clock (CLK). The output enables (1OEAB, 1OEBA, 2OEAB, and 2OEBA) control byte 1 and byte 2 data for the A-to-B and B-to-A directions, respectively. Note that CLK is common to both directions and both 8-bit words. OE also is common and disables all I/O ports simultaneously.

For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB transitions low, the A data is latched independent of CLK high or low. If LEAB is low, the A data is registered on the CLK low-to-high transition. When OEAB is low, the outputs are active. With OEAB high, the outputs are in the high-impedance state.

The data flow for the B-to-A direction is identical, except OEBA, LEBA, and CLK are used.

## Function Tables

FUNCTION†					
INPUTS				OUTPUT B	MODE
OEAB	LEAB	CLK	A		
H	X	X	X	Z	Isolation
L	L	H	X	B <sub>0</sub> ‡	Latched storage of A data
L	L	L	X	B <sub>0</sub> §	
L	H	X	L	L	True transparent
L	H	X	H	H	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

† A-to-B data flow is shown. B-to-A flow is similar, but uses OEBA, LEBA, and CLK. The condition when OEAB and OEBA are both low at the same time is not recommended.

‡ Output level before the indicated steady-state input conditions were established, provided that CLK was high before LEAB went low

§ Output level before the indicated steady-state input conditions were established

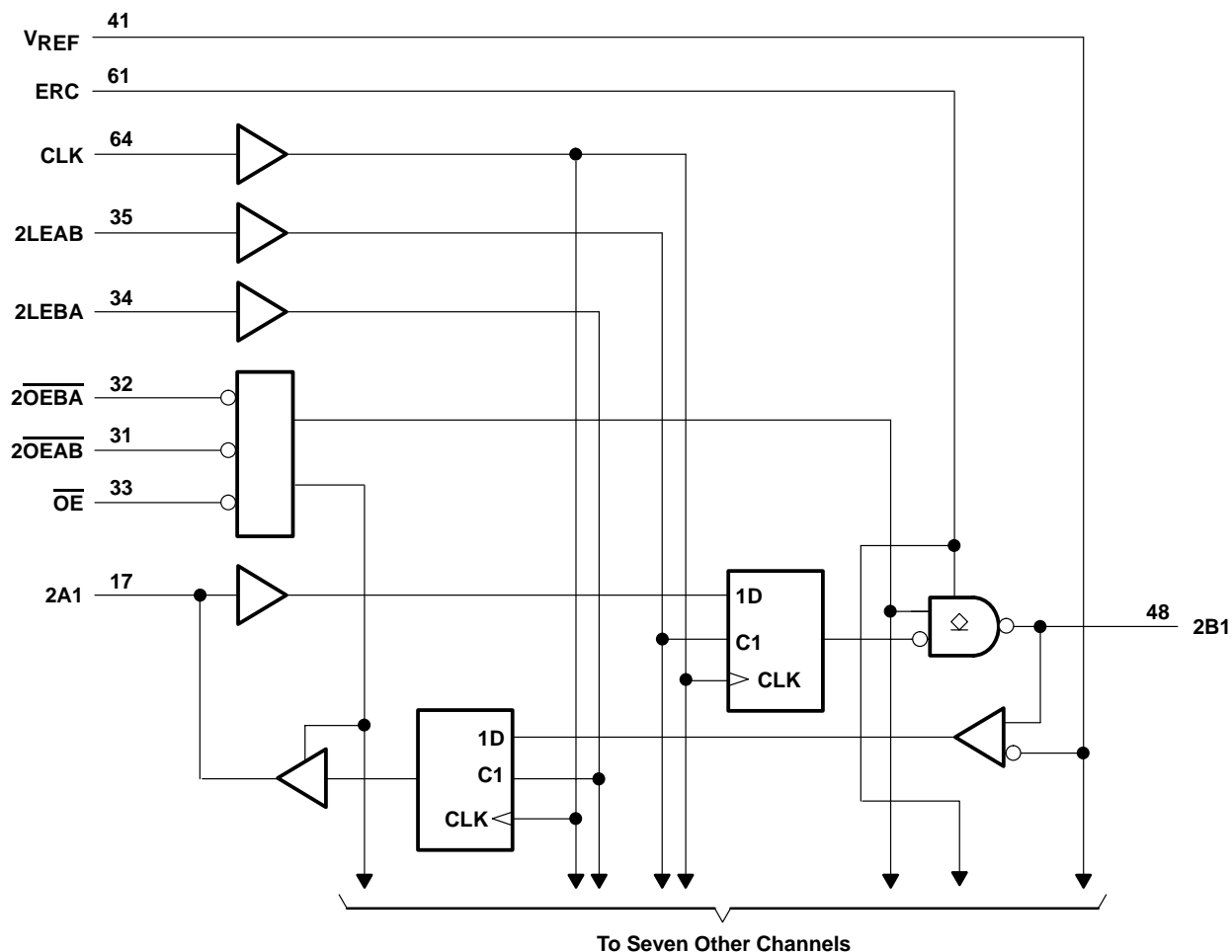
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**OUTPUT ENABLE**

† This condition is not recommended.

INPUT ERC		OUTPUT B-PORT EDGE RATE
LOGIC LEVEL	NOMINAL VOLTAGE	
H	V <sub>CC</sub>	Slow
L	GND	Fast

logic diagram (positive logic) (continued)



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ and BIAS $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1): A port, ERC, and control inputs	–0.5 V to 7 V
B port and $V_{REF}$	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$	
(see Note 1): A port	–0.5 V to 7 V
B port	–0.5 V to 4.6 V
Current into any output in the low state, $I_O$ : A port	48 mA
B port	200 mA
Current into any A port output in the high state, $I_O$ (see Note 2)	48 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	55°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.



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**recommended operating conditions (see Notes 4 through 7)**

			MIN	NOM	MAX	UNIT
V <sub>CC</sub> , BIAS V <sub>CC</sub>	Supply voltage		3.15	3.3	3.45	V
V <sub>TT</sub>	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V <sub>REF</sub>	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V <sub>I</sub>	Input voltage	B port	V <sub>TT</sub>			V
		Except B port	V <sub>CC</sub> 5.5			
V <sub>IH</sub>	High-level input voltage	B port	V <sub>REF</sub> +0.05			V
		ERC	V <sub>CC</sub> −0.6	V <sub>CC</sub>	5.5	
		Except B port and ERC	2			
V <sub>IL</sub>	Low-level input voltage	B port	V <sub>REF</sub> −0.05			V
		ERC	GND 0.6			
		Except B port and ERC	0.8			
I <sub>IK</sub>	Input clamp current		−18			mA
I <sub>OH</sub>	High-level output current	A port	−24			mA
I <sub>OL</sub>	Low-level output current	A port	24			mA
		B port	100			
Δt/Δv	Input transition rise or fall rate	Outputs enabled	10			ns/V
Δt/ΔV <sub>CC</sub>	Power-up ramp rate		20			μs/V
T <sub>A</sub>	Operating free-air temperature		−40 85			°C

- NOTES:
- All unused control and B-port inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
  - Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS  $V_{CC} = 3.3$  V first, I/O second, and  $V_{CC} = 3.3$  V last, because the BIAS  $V_{CC}$  precharge circuitry is disabled when any  $V_{CC}$  pin is connected. The control and  $V_{REF}$  inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
  - $V_{TT}$  and  $R_{TT}$  can be adjusted to accommodate backplane impedances if the dc recommended  $I_{OL}$  ratings are not exceeded.
  - $V_{REF}$  can be adjusted to optimize noise margins, but normally is two-thirds  $V_{TT}$ . TI-OPC circuitry is enabled in the A-to-B direction and is activated when  $V_{TT} > 0.7$  V above  $V_{REF}$ . If operated in the A-to-B direction,  $V_{REF}$  should be set to within 0.6 V of  $V_{TT}$  to minimize current drain.



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**electrical characteristics over recommended operating free-air temperature range for GTLP (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.15 \text{ V}$ ,	$I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$	A port	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$ ,	$I_{OH} = -100 \mu\text{A}$	$V_{CC}-0.2$			V
		$V_{CC} = 3.15 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2.4			
			$I_{OH} = -24 \text{ mA}$	2			
$V_{OL}$	A port	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$ ,	$I_{OL} = 100 \mu\text{A}$			0.2	V
		$V_{CC} = 3.15 \text{ V}$	$I_{OL} = 12 \text{ mA}$			0.4	
			$I_{OL} = 24 \text{ mA}$			0.5	
	B port	$V_{CC} = 3.15 \text{ V}$	$I_{OL} = 10 \text{ mA}$			0.2	
			$I_{OL} = 64 \text{ mA}$			0.4	
			$I_{OL} = 100 \text{ mA}$			0.55	
$I_I$	Control inputs	$V_{CC} = 3.45 \text{ V}$ ,	$V_I = 0 \text{ or } 5.5 \text{ V}$			$\pm 10$	$\mu\text{A}$
$I_{OZH}^\ddagger$	A port	$V_{CC} = 3.45 \text{ V}$	$V_O = V_{CC}$			10	$\mu\text{A}$
	B port		$V_O = 1.5 \text{ V}$			10	
$I_{OZL}^\ddagger$	A and B ports	$V_{CC} = 3.45 \text{ V}$ ,	$V_O = \text{GND}$			-10	$\mu\text{A}$
$I_{BHL}^\S$	A port	$V_{CC} = 3.15 \text{ V}$ ,	$V_I = 0.8 \text{ V}$	75			$\mu\text{A}$
$I_{BHH}^\P$	A port	$V_{CC} = 3.15 \text{ V}$ ,	$V_I = 2 \text{ V}$	-75			$\mu\text{A}$
$I_{BHLO}^\#$	A port	$V_{CC} = 3.45 \text{ V}$ ,	$V_I = 0 \text{ to } V_{CC}$	500			$\mu\text{A}$
$I_{BHLO}^\parallel$	A port	$V_{CC} = 3.45 \text{ V}$ ,	$V_I = 0 \text{ to } V_{CC}$	-500			$\mu\text{A}$
$I_{CC}$	A or B port	$V_{CC} = 3.45 \text{ V}$ , $I_O = 0$ , $V_I$ (A-port or control input) = $V_{CC}$ or GND, $V_I$ (B port) = $V_{TT}$ or GND	Outputs high			40	mA
			Outputs low			40	
			Outputs disabled			40	
$\Delta I_{CC}^\star$		$V_{CC} = 3.45 \text{ V}$ , One A-port or control input at $V_{CC} - 0.6 \text{ V}$ , Other A-port or control inputs at $V_{CC}$ or GND				1.5	mA
$C_i$	Control inputs	$V_I = 3.15 \text{ V or } 0$			4.5	6.5	pF
$C_{io}$	A port	$V_O = 3.15 \text{ V or } 0$			6.5	7.5	pF
	B port	$V_O = 1.5 \text{ V or } 0$			8.5	10.5	

† All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameters  $I_{OZH}$  and  $I_{OZL}$  include the input leakage current.

§ The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL\text{max}}$ .  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL\text{max}}$ .

¶ The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH\text{min}}$ .  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH\text{min}}$ .

# An external driver must source at least  $I_{BHLO}$  to switch this node from low to high.

|| An external driver must sink at least  $I_{BHLO}$  to switch this node from high to low.

\* This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

**hot-insertion specifications for A port over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0$ ,	BIAS $V_{CC} = 0$ ,	$V_I \text{ or } V_O = 0 \text{ to } 5.5 \text{ V}$		10	$\mu\text{A}$
$I_{OZPU}$	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$ ,	$V_O = 0.5 \text{ V to } 3 \text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5 \text{ V to } 0$ ,	$V_O = 0.5 \text{ V to } 3 \text{ V}$ ,	$\overline{OE} = 0$		$\pm 30$	$\mu\text{A}$





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**live-insertion specifications for B port over recommended operating free-air temperature range**

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
$I_{off}$	$V_{CC} = 0$ ,	BIAS $V_{CC} = 0$ ,	$V_I$ or $V_O = 0$ to 1.5 V		10	$\mu A$
$I_{OZPU}$	$V_{CC} = 0$ to 1.5 V,	BIAS $V_{CC} = 0$ ,	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		$\pm 30$	$\mu A$
$I_{OZPD}$	$V_{CC} = 1.5$ V to 0,	BIAS $V_{CC} = 0$ ,	$V_O = 0.5$ V to 1.5 V, $\overline{OE} = 0$		$\pm 30$	$\mu A$
$I_{CC}$ (BIAS $V_{CC}$ )	$V_{CC} = 0$ to 3.15 V	BIAS $V_{CC} = 3.15$ V to 3.45 V,	$V_O$ (B port) = 0 to 1.5 V		5	mA
	$V_{CC} = 3.15$ V to 3.45 V				10	$\mu A$
$V_O$	$V_{CC} = 0$ ,	BIAS $V_{CC} = 3.3$ V	$I_O = 0$	0.95	1.05	V
$I_O$	$V_{CC} = 0$ ,	BIAS $V_{CC} = 3.15$ V to 3.45 V,	$V_O$ (B port) = 0.6 V	-1		$\mu A$

**timing requirements over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5$  V and  $V_{REF} = 1$  V for GTLP (unless otherwise noted)**

		MIN	MAX	UNIT
$f_{clock}$	Clock frequency		175	MHz
$t_w$	Pulse duration	LEAB or LEBA high	3	ns
		CLK high or low	3	
$t_{su}$	Setup time	A before CLK	3	ns
		B before CLK	3	
		A before LEAB $\downarrow$ , CLK = don't care	2.5	
		B before LEBA $\downarrow$ , CLK = don't care	2.5	
$t_h$	Hold time	A after CLK	0.5	ns
		B after CLK	0.5	
		A after LEAB $\downarrow$ , CLK = don't care	0.5	
		B after LEBA $\downarrow$ , CLK = don't care	0.5	



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	MIN	TYP‡	MAX	UNIT
f <sub>max</sub>				175			MHz
t <sub>PLH</sub>	A	B	Slow	3.5	7.7		ns
t <sub>PHL</sub>				2.4	6.3		
t <sub>PLH</sub>	A	B	Fast	2	6.3		ns
t <sub>PHL</sub>				2	5.9		
t <sub>PLH</sub>	LEAB	B	Slow	3.5	7.8		ns
t <sub>PHL</sub>				2.7	6.4		
t <sub>PLH</sub>	LEAB	B	Fast	2	6.4		ns
t <sub>PHL</sub>				2	6		
t <sub>PLH</sub>	CLK	B	Slow	4.7	8		ns
t <sub>PHL</sub>				2.7	6.4		
t <sub>PLH</sub>	CLK	B	Fast	3.6	6.8		ns
t <sub>PHL</sub>				2	6.1		
t <sub>en</sub>	$\overline{OE}$	B	Slow	3.5	7.3		ns
t <sub>dis</sub>				3.5	7		
t <sub>en</sub>	$\overline{OE}$	B	Fast	2	6		ns
t <sub>dis</sub>				2	6.6		
t <sub>en</sub>	$\overline{OEAB}$	B	Slow	3.5	7.4		ns
t <sub>dis</sub>				3.5	7		
t <sub>en</sub>	$\overline{OEAB}$	B	Fast	2	6.1		ns
t <sub>dis</sub>				2	6.3		
t <sub>r</sub>	Rise time, B outputs (20% to 80%)		Slow	2.6			ns
			Fast	1.5			
t <sub>f</sub>	Fall time, B outputs (80% to 20%)		Slow	3			ns
			Fast	2.2			
t <sub>PLH</sub>	B	A	–	1.5	5.5		ns
t <sub>PHL</sub>				1.5	5.5		
t <sub>PLH</sub>	LEBA	A	–	1.3	5.2		ns
t <sub>PHL</sub>				1	5		
t <sub>PLH</sub>	CLK	A	–	1.2	6.3		ns
t <sub>PHL</sub>				1	5		
t <sub>en</sub>	$\overline{OE}$	A	–	1.5	5.6		ns
t <sub>dis</sub>				1.5	6.1		
t <sub>en</sub>	$\overline{OEBA}$	A	–	1.2	5.4		ns
t <sub>dis</sub>				2	6.1		

† Slow (ERC =  $V_{CC}$ ) and Fast (ERC = GND)

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

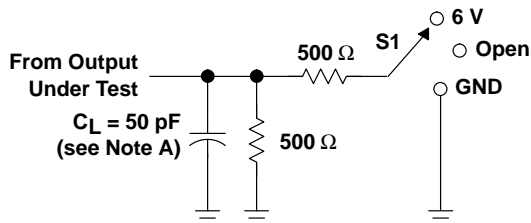
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## 16-BIT LVTTTL-TO-GTLP ADJUSTABLE-EDGE-RATE

### UNIVERSAL BUS TRANSCEIVER

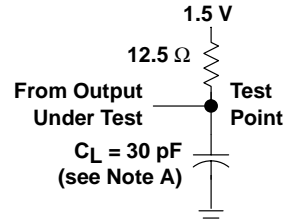
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#### PARAMETER MEASUREMENT INFORMATION

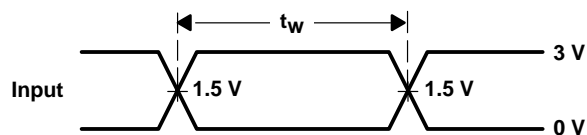


LOAD CIRCUIT FOR A OUTPUTS

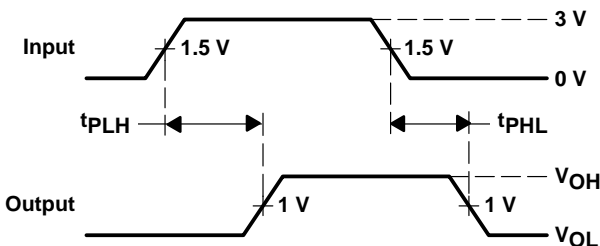
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



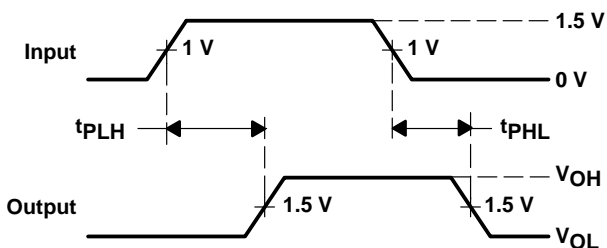
LOAD CIRCUIT FOR B OUTPUTS



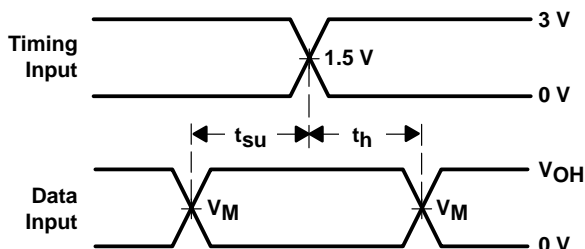
VOLTAGE WAVEFORMS  
PULSE DURATION



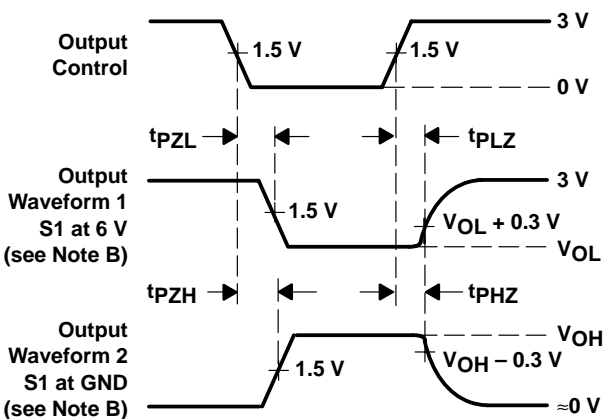
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(A port to B port)



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
(B port to A port)



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES  
( $V_M = 1.5 \text{ V}$  for A port and  $1 \text{ V}$  for B port)  
( $V_{OH} = 3 \text{ V}$  for A port and  $1.5 \text{ V}$  for B port)



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
(A port)

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\approx 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \approx 2 \text{ ns}$ ,  $t_f \approx 2 \text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

# SN74GTLP1655

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#### DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See [www.ti.com/sc/gt1p](http://www.ti.com/sc/gt1p) for more information.

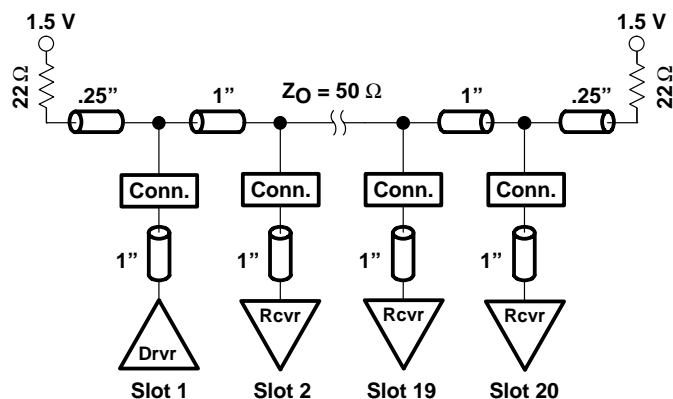


Figure 2. High-Drive Test Backplane

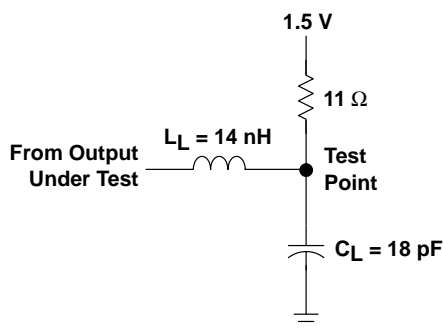


Figure 3. High-Drive RLC Network

**SN74GTLP1655**  
**16-BIT LVTTL-TO-GTLP ADJUSTABLE-EDGE-RATE**  
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $V_{TT} = 1.5\text{ V}$  and  $V_{REF} = 1\text{ V}$  for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE†	TYP‡	UNIT
tPLH	A	B	Slow	5	ns
tPHL				5	
tPLH	A	B	Fast	3.8	ns
tPHL				3.8	
tPLH	LEAB	B	Slow	4.9	ns
tPHL				4.9	
tPLH	LEAB	B	Fast	3.9	ns
tPHL				3.9	
tPLH	CLK	B	Slow	4.8	ns
tPHL				4.8	
tPLH	CLK	B	Fast	3.7	ns
tPHL				3.7	
ten	OEAB or OE	B	Slow	4.9	ns
tdis				4.7	
ten	OEAB or OE	B	Fast	3.5	ns
tdis				4.1	
tr	Rise time, B outputs (20% to 80%)		Slow	2	ns
			Fast	1.2	
tf	Fall time, B outputs (80% to 20%)		Slow	2.5	ns
			Fast	1.8	

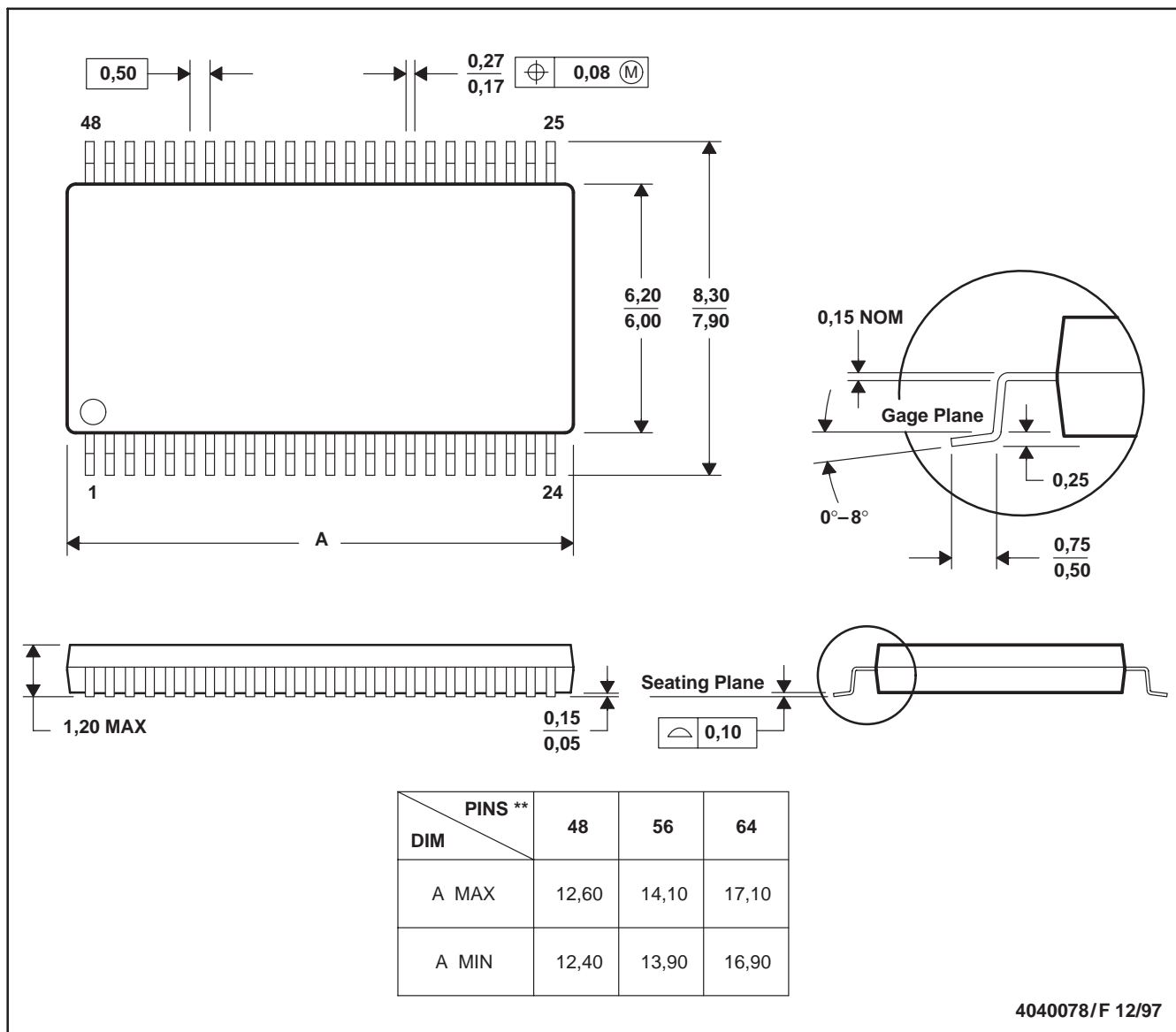
† Slow (ERC =  $V_{CC}$ ) and Fast (ERC = GND)

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ . All values are derived from TI-SPICE models.

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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