

# 3.3 V, 2.5 Gb/s Dual AnyLevel™ to LVDS Receiver/Driver/Buffer/ Translator with Internal Input Termination

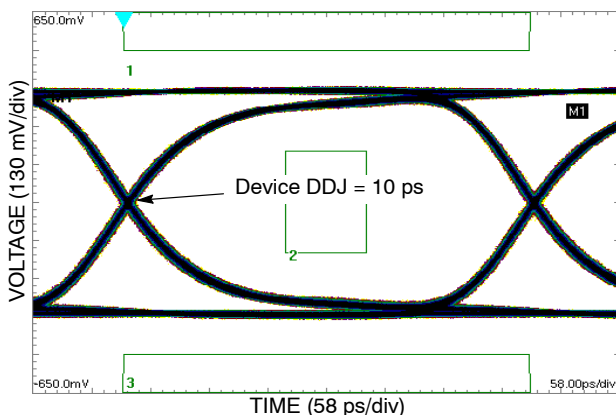
## NB4N527S

NB4N527S is a clock or data Receiver/Driver/Buffer/Translator capable of translating AnyLevel™ input signal (LVPECL, CML, HSTL, LVDS, or LVTTL/LVCMOS) to LVDS. Depending on the distance, noise immunity of the system design, and transmission line media, this device will receive, drive or translate data or clock signals up to 2.5 Gb/s or 1.5 GHz, respectively.

The NB4N527S has a wide input common mode range of  $GND + 50\text{ mV}$  to  $V_{CC} - 50\text{ mV}$  combined with two  $50\ \Omega$  internal termination resistors is ideal for translating differential or single-ended data or clock signals to 350 mV typical LVDS output levels without use of any additional external components (Figure 6).

The device is offered in a small 3 mm x 3 mm QFN-16 package. NB4N527S is targeted for data, wireless and telecom applications as well as high speed logic interface where jitter and package size are main requirements. Application notes, models, and support documentation are available on [www.onsemi.com](http://www.onsemi.com).

- Maximum Input Clock Frequency up to 1.5 GHz
- Maximum Input Data Rate up to 2.5 Gb/s (Figure 5)
- 470 ps Maximum Propagation Delay\
- 1 ps Maximum RMS Jitter
- 140 ps Maximum Rise/Fall Times
- Single Power Supply;  $V_{CC} = 3.3\text{ V} \pm 10\%$
- Temperature Compensated TIA/EIA-644 Compliant LVDS Outputs
- Internal  $50\ \Omega$  Termination Resistor per Input Pin
- $GND + 50\text{ mV}$  to  $V_{CC} - 50\text{ mV}$   $V_{CMR}$  Range
- These are Pb-Free Devices

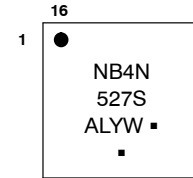


**Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23}-1$  ( $V_{INPP} = 400\text{ mV}$ ; Input Signal DDJ = 14 ps)**



QFN-16  
MN SUFFIX  
CASE 485G

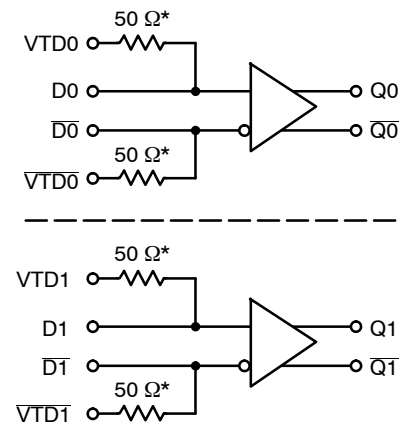
### MARKING DIAGRAM\*



|   |                     |
|---|---------------------|
| A | = Assembly Location |
| L | = Wafer Lot         |
| Y | = Year              |
| W | = Work Week         |
| ▪ | = Pb-Free Package   |

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note [AND8002/D](#).



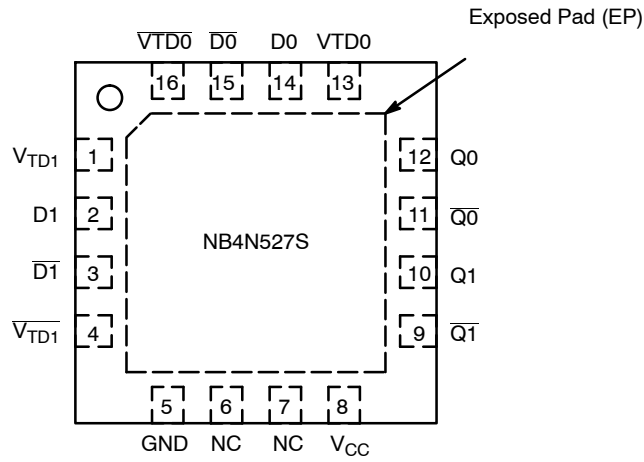
**Figure 1. Functional Block Diagram**

\* $R_{TIN}$

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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**Figure 3. Pin Configuration** (Top View)

**Table 1. PIN DESCRIPTION**

| Pin  | Name              | I/O                                     | Description                                                                                                                                                                                                           |
|------|-------------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | VTD1              | –                                       | Internal 50 $\Omega$ termination pin for D1. ( $R_{TIN}$ )                                                                                                                                                            |
| 2    | D1                | LVPECL, CML, LVDS, LVCMOS, LVTTTL, HSTL | Noninverted differential clock/data D1 input (Note 1).                                                                                                                                                                |
| 3    | $\overline{D1}$   | LVPECL, CML, LVDS, LVCMOS, LVTTTL, HSTL | Inverted differential clock/data $\overline{D1}$ input (Note 1).                                                                                                                                                      |
| 4    | $\overline{VTD1}$ | –                                       | Internal 50 $\Omega$ termination pin for $\overline{D1}$ . ( $R_{TIN}$ )                                                                                                                                              |
| 5    | GND               | –                                       | 0 V. Ground.                                                                                                                                                                                                          |
| 6, 7 | NC                |                                         | No connect.                                                                                                                                                                                                           |
| 8    | $V_{CC}$          |                                         | Positive Supply Voltage.                                                                                                                                                                                              |
| 9    | $\overline{Q1}$   | LVDS Output                             | Inverted D1 output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.                                                                                                        |
| 10   | Q1                | LVDS Output                             | Noninverted D1 output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.                                                                                                     |
| 11   | $\overline{Q0}$   | LVDS Output                             | Inverted D0 output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.                                                                                                        |
| 12   | Q0                | LVDS Output                             | Noninverted D0 output. Typically loaded with 100 $\Omega$ receiver termination resistor across differential pair.                                                                                                     |
| 13   | VTD0              | –                                       | Internal 50 $\Omega$ termination pin for D0.                                                                                                                                                                          |
| 14   | D0                | LVPECL, CML, LVDS, LVCMOS, LVTTTL, HSTL | Noninverted differential clock/data D0 input (Note 1).                                                                                                                                                                |
| 15   | $\overline{D0}$   | LVPECL, CML, LVDS, LVCMOS, LVTTTL, HSTL | Inverted differential clock/data $\overline{D0}$ input (Note 1).                                                                                                                                                      |
| 16   | $\overline{VTD0}$ | –                                       | Internal 50 $\Omega$ termination pin for $\overline{D0}$ .                                                                                                                                                            |
| EP   |                   |                                         | Exposed pad. EP on the package bottom is thermally connected to the die improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be soldered to GND on the PCB. |

1. In the differential configuration when the input termination pins(VTD0/ $\overline{VTD0}$ , VTD1/ $\overline{VTD1}$ ) are connected to a common termination voltage or left open, and if no signal is applied on D0/ $\overline{D0}$ , D1/ $\overline{D1}$  input, then the device will be susceptible to self-oscillation.

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**Table 2. ATTRIBUTES**

| Characteristics                                        | Value                                                     |
|--------------------------------------------------------|-----------------------------------------------------------|
| Moisture Sensitivity (Note 2)                          | Level 1                                                   |
| Flammability Rating                                    | Oxygen Index: 28 to 34<br>UL 94 V-0 @ 0.125 in            |
| ESD Protection                                         | Human Body Model<br>Machine Model<br>Charged Device Model |
| Transistor Count                                       | 281                                                       |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |                                                           |

2. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter                                                                                             | Condition 1                             | Condition 2                      | Rating       | Unit         |
|------------------|-------------------------------------------------------------------------------------------------------|-----------------------------------------|----------------------------------|--------------|--------------|
| V <sub>CC</sub>  | Positive Power Supply                                                                                 | GND = 0 V                               |                                  | 3.8          | V            |
| V <sub>I</sub>   | Positive Input                                                                                        | GND = 0 V                               | V <sub>I</sub> = V <sub>CC</sub> | 3.8          | V            |
| I <sub>IN</sub>  | Input Current Through R <sub>T</sub> (50 Ω Resistor)                                                  | Static<br>Surge                         |                                  | 35<br>70     | mA<br>mA     |
| I <sub>OSC</sub> | Output Short Circuit Current<br>Line-to-Line (Q to $\bar{Q}$ )<br>Line-to-End (Q or $\bar{Q}$ to GND) | Q or $\bar{Q}$ to GND<br>Q to $\bar{Q}$ | Continuous<br>Continuous         | 12<br>24     | mA           |
| T <sub>A</sub>   | Operating Temperature Range                                                                           | QFN-16                                  |                                  | -40 to +85   | °C           |
| T <sub>stg</sub> | Storage Temperature Range                                                                             |                                         |                                  | -65 to +150  | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) (Note 3)                                                     | 0 lfpm<br>500 lfpm                      | QFN-16<br>QFN-16                 | 41.6<br>35.2 | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)                                                                 | 1S2P (Note 3)                           | QFN-16                           | 4.0          | °C/W         |
| T <sub>sol</sub> | Wave Solder<br>Pb<br>Pb-Free                                                                          |                                         |                                  | 265<br>265   | °C           |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 4. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS**  $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ 

| Symbol   | Characteristic                | Min | Typ | Max | Unit |
|----------|-------------------------------|-----|-----|-----|------|
| $I_{CC}$ | Power Supply Current (Note 8) |     | 40  | 53  | mA   |

**DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED** (Figures 11, 12, 16, and 18)

|          |                                                  |                |  |                |    |
|----------|--------------------------------------------------|----------------|--|----------------|----|
| $V_{th}$ | Input Threshold Reference Voltage Range (Note 7) | $GND + 100$    |  | $V_{CC} - 100$ | mV |
| $V_{IH}$ | Single-ended Input HIGH Voltage                  | $V_{th} + 100$ |  | $V_{CC}$       | mV |
| $V_{IL}$ | Single-ended Input LOW Voltage                   | $GND$          |  | $V_{th} - 100$ | mV |

**DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Figures 7, 8, 9, 10, 17, and 19)

|           |                                                      |            |    |                |          |
|-----------|------------------------------------------------------|------------|----|----------------|----------|
| $V_{IHD}$ | Differential Input HIGH Voltage                      | 100        |    | $V_{CC}$       | mV       |
| $V_{ILD}$ | Differential Input LOW Voltage                       | $GND$      |    | $V_{CC} - 100$ | mV       |
| $V_{CMR}$ | Input Common Mode Range (Differential Configuration) | $GND + 50$ |    | $V_{CC} - 50$  | mV       |
| $V_{ID}$  | Differential Input Voltage ( $V_{IHD} - V_{ILD}$ )   | 100        |    | $V_{CC}$       | mV       |
| $R_{TIN}$ | Internal Input Termination Resistor                  | 40         | 50 | 60             | $\Omega$ |

**LVDS OUTPUTS** (Note 4)

|                 |                                                                          |      |      |      |    |
|-----------------|--------------------------------------------------------------------------|------|------|------|----|
| $V_{OD}$        | Differential Output Voltage                                              | 250  |      | 450  | mV |
| $\Delta V_{OD}$ | Change in Magnitude of $V_{OD}$ for Complementary Output States (Note 9) | 0    | 1    | 25   | mV |
| $V_{OS}$        | Offset Voltage (Figure 15)                                               | 1125 |      | 1375 | mV |
| $\Delta V_{OS}$ | Change in Magnitude of $V_{OS}$ for Complementary Output States (Note 9) | 0    | 1    | 25   | mV |
| $V_{OH}$        | Output HIGH Voltage (Note 5)                                             |      | 1425 | 1600 | mV |
| $V_{OL}$        | Output LOW Voltage (Note 6)                                              | 900  | 1075 |      | mV |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

4. LVDS outputs require  $100\ \Omega$  receiver termination resistor between differential pair. See Figure 14.
5.  $V_{OHmax} = V_{OSmax} + \frac{1}{2} V_{ODmax}$ .
6.  $V_{OLmax} = V_{OSmin} - \frac{1}{2} V_{ODmax}$ .
7.  $V_{th}$  is applied to the complementary input when operating in single-ended mode.
8. Input termination pins open,  $Dx/Dx$  at the DC level within  $V_{CMR}$  and output pins loaded with  $R_L = 100\ \Omega$  across differential.
9. Parameter guaranteed by design verification not tested in production.

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**Table 5. AC CHARACTERISTICS**  $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ ,  $GND = 0 \text{ V}$ ; (Note 10)

| Symbol                   | Characteristic                                                                                                                                                                                                                                                       | -40°C      |                                  |                                | 25°C       |                                  |                                | 85°C       |                                  |                                | Unit |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----------------------------------|--------------------------------|------------|----------------------------------|--------------------------------|------------|----------------------------------|--------------------------------|------|
|                          |                                                                                                                                                                                                                                                                      | Min        | Typ                              | Max                            | Min        | Typ                              | Max                            | Min        | Typ                              | Max                            |      |
| $V_{OUTPP}$              | Output Voltage Amplitude (@ $V_{INPPmin}$ ) $f_{in} \leq 1.0 \text{ GHz}$<br>(Figure 4) $f_{in} = 1.5 \text{ GHz}$                                                                                                                                                   | 220<br>200 | 350<br>300                       |                                | 220<br>200 | 350<br>300                       |                                | 220<br>200 | 350<br>300                       |                                | mV   |
| $f_{DATA}$               | Maximum Operating Data Rate                                                                                                                                                                                                                                          | 1.5        | 2.5                              |                                | 1.5        | 2.5                              |                                | 1.5        | 2.5                              |                                | Gb/s |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Differential Input to Differential Output<br>Propagation Delay                                                                                                                                                                                                       | 270        | 370                              | 470                            | 270        | 370                              | 470                            | 270        | 370                              | 470                            | ps   |
| $t_{SKEW}$               | Duty Cycle Skew (Note 11)<br>Within Device Skew (Note 17)<br>Device-to-Device Skew (Note 15)                                                                                                                                                                         |            | 8<br>5<br>30                     | 45<br>25<br>100                |            | 8<br>5<br>30                     | 45<br>25<br>100                |            | 8<br>5<br>30                     | 45<br>25<br>100                | ps   |
| $t_{JITTER}$             | RMS Random Clock Jitter (Note 13) $f_{in} = 1.0 \text{ GHz}$<br>$f_{in} = 1.5 \text{ GHz}$<br>Deterministic Jitter (Note 14) $f_{DATA} = 622 \text{ Mb/s}$<br>$f_{DATA} = 1.5 \text{ Gb/s}$<br>$f_{DATA} = 2.488 \text{ Gb/s}$<br>Crosstalk Induced Jitter (Note 16) |            | 0.5<br>0.5<br>6<br>7<br>10<br>20 | 1<br>1<br>20<br>20<br>25<br>40 |            | 0.5<br>0.5<br>6<br>7<br>10<br>20 | 1<br>1<br>20<br>20<br>25<br>40 |            | 0.5<br>0.5<br>6<br>7<br>10<br>20 | 1<br>1<br>20<br>20<br>25<br>40 | ps   |
| $V_{INPP}$               | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 12)                                                                                                                                                                                            | 100        |                                  | $V_{CC} - GND$                 | 100        |                                  | $V_{CC} - GND$                 | 100        |                                  | $V_{CC} - GND$                 | mV   |
| $t_r$<br>$t_f$           | Output Rise/Fall Times @ 250 MHz<br>(20% – 80%) $Q, \bar{Q}$                                                                                                                                                                                                         | 60         | 100                              | 140                            | 60         | 100                              | 140                            | 60         | 100                              | 140                            | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

10. Measured by forcing  $V_{INPPmin}$  with 50% duty cycle clock source and  $V_{CC} - 1400 \text{ mV}$  offset. All loading with an external  $R_L = 100 \Omega$  across "D" and "D" of the receiver. Input edge rates 150 ps (20%–80%).

11. See Figure 13 differential measurement of  $t_{skew} = |t_{PLH} - t_{PHL}|$  for a nominal 50% differential clock input waveform @ 250 MHz.

12. Input voltage swing is a single-ended measurement operating in differential mode.

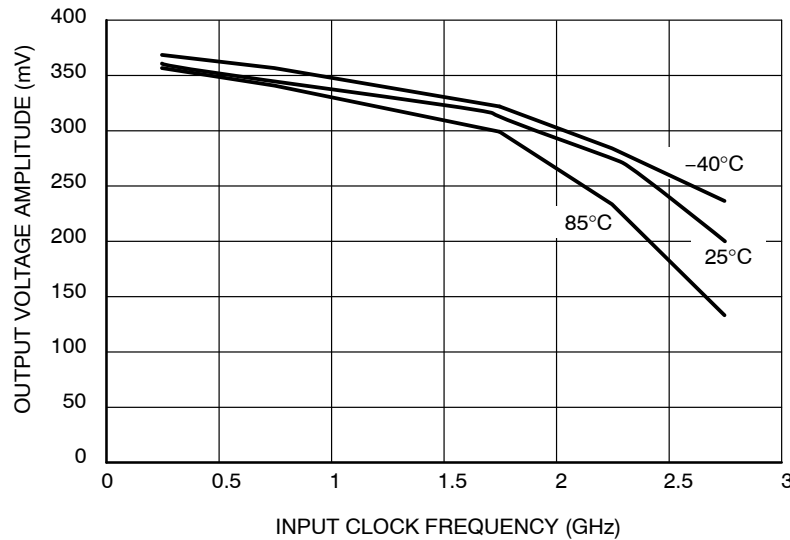
13. RMS jitter with 50% duty cycle input clock signal.

14. Deterministic jitter with input NRZ data at PRBS  $2^{23}-1$  and K28.5.

15. Skew is measured between outputs under identical transition @ 250 MHz.

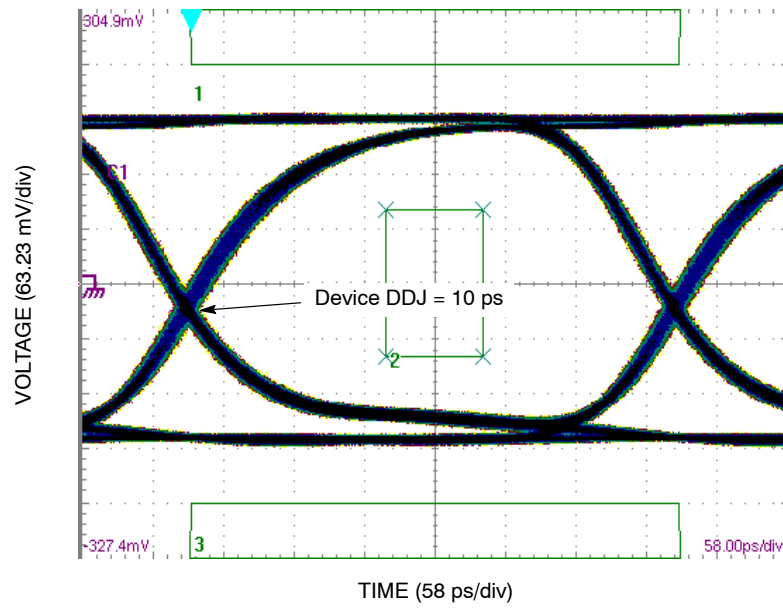
16. Crosstalk induced jitter is the additive deterministic jitter to channel one with channel two active both running at 622 Gb/s PRBS  $2^{23}-1$  as an asynchronous signals.

17. The worst case condition between  $Q0/\bar{Q}0$  and  $Q1/\bar{Q}1$  from either  $D0/\bar{D}0$  or  $D1/\bar{D}1$ , when both outputs have the same transition.

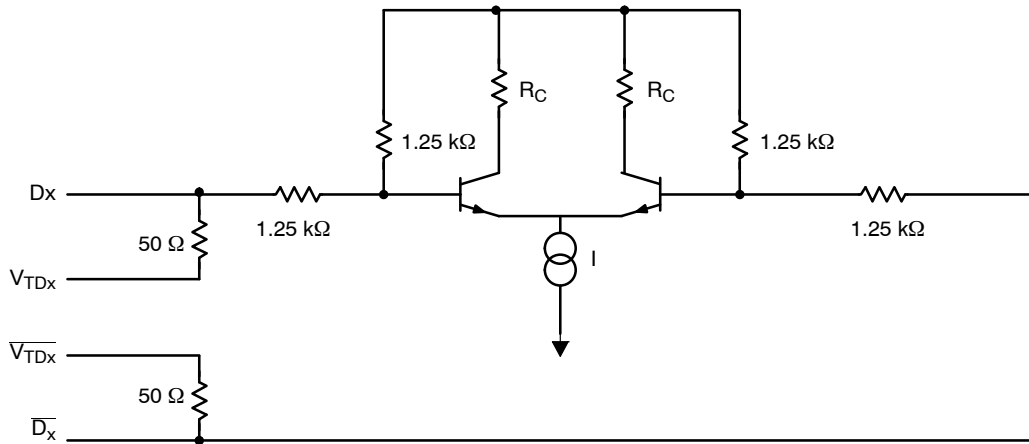


**Figure 4. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Input Clock Frequency ( $f_{in}$ ) and Temperature (@  $V_{CC} = 3.3 \text{ V}$ )**

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**Figure 5. Typical Output Waveform at 2.488 Gb/s with PRBS  $2^{23}-1$  and OC48 mask ( $V_{INPP} = 100$  mV; Input Signal DDJ = 14 ps)**



**Figure 6. Input Structure**

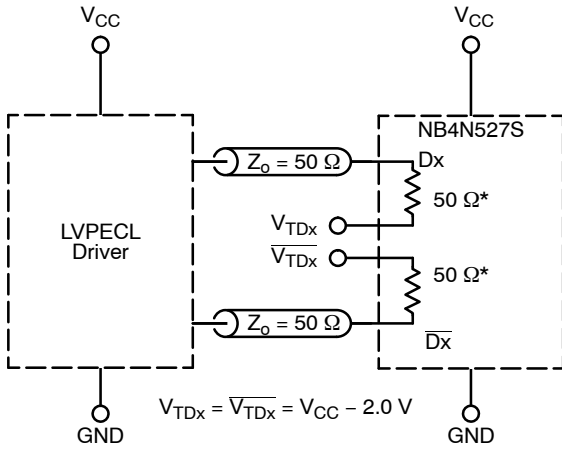


Figure 7. LVPECL Interface

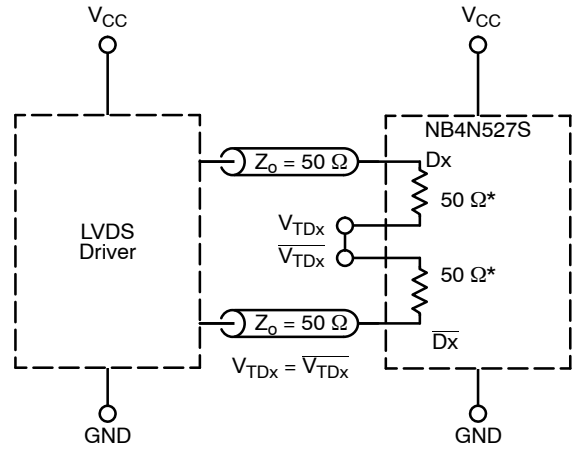


Figure 8. LVDS Interface

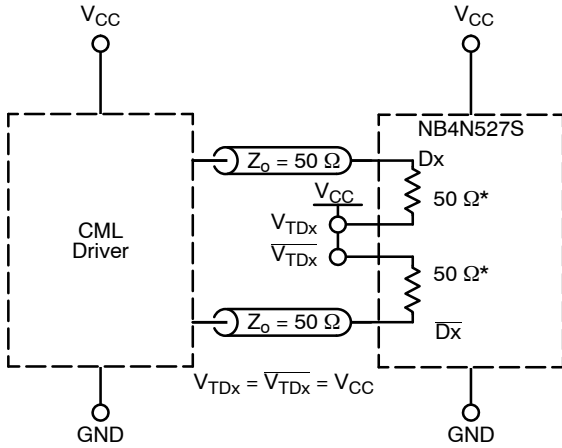


Figure 9. Standard 50 Ω Load CML Interface

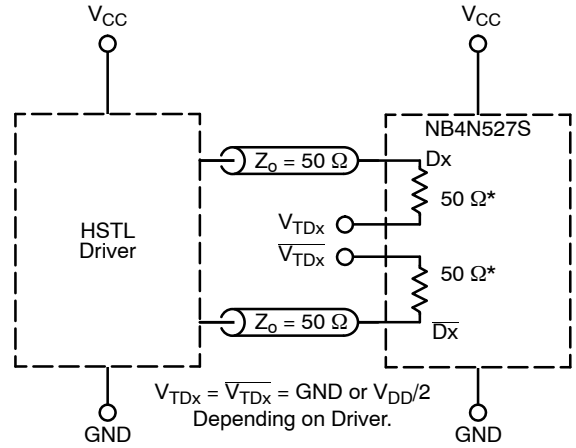
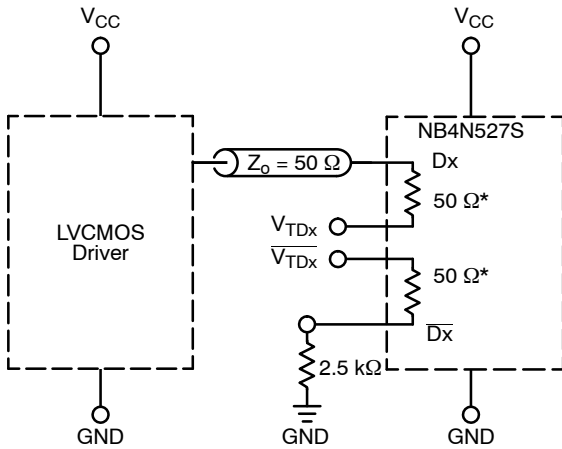
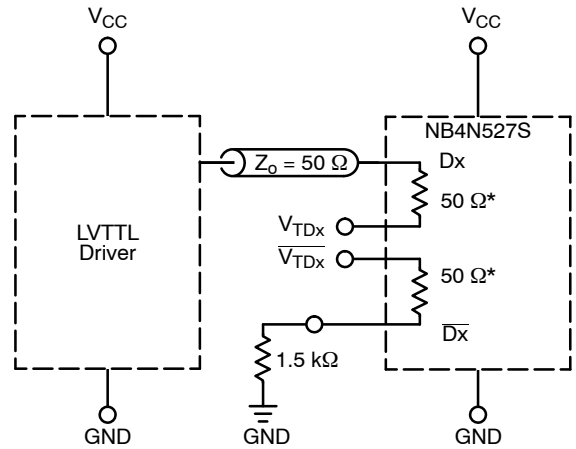


Figure 10. HSTL Interface



$$V_{TDx} = \overline{V_{TDx}} = \text{OPEN}$$

Figure 11. LVCMOS Interface



$$V_{TDx} = \text{OPEN}$$

Figure 12. LVTTTL Interface

\*R<sub>TIN</sub>, Internal Input Termination Resistor.

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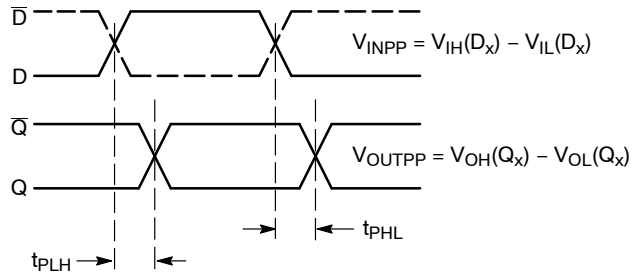


Figure 13. AC Reference Measurement

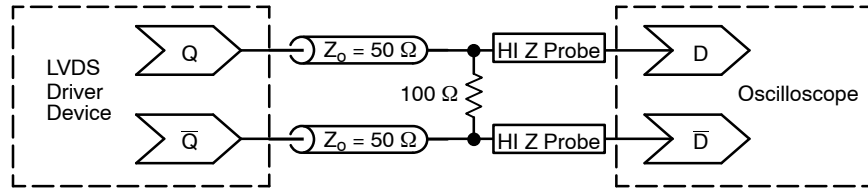


Figure 14. Typical LVDS Termination for Output Driver and Device Evaluation

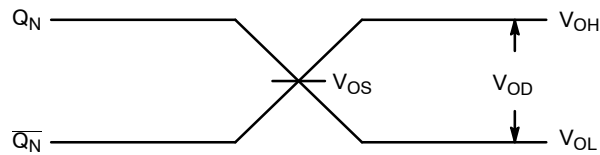


Figure 15. LVDS Output

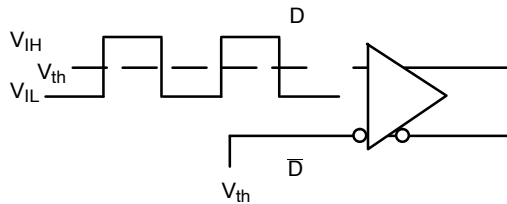


Figure 16. Differential Input Driven Single-Ended

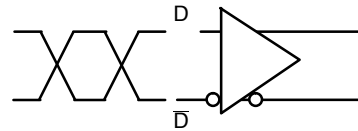


Figure 17. Differential Inputs Driven Differentially

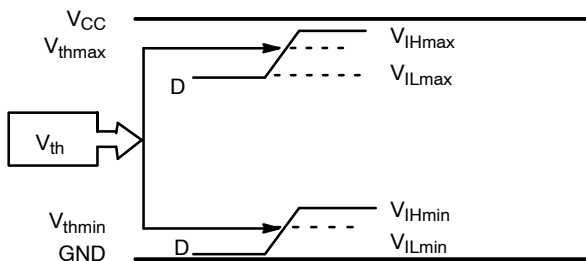


Figure 18.  $V_{th}$  Diagram

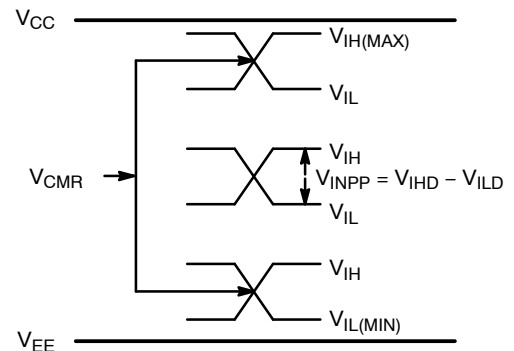


Figure 19.  $V_{CMR}$  Diagram

## NB4N527S

### ORDERING INFORMATION

| Device        | Package             | Shipping <sup>†</sup> |
|---------------|---------------------|-----------------------|
| NB4N527SMNG   | QFN-16<br>(Pb-Free) | 123 Units / Rail      |
| NB4N527SMNR2G | QFN-16<br>(Pb-Free) | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

AnyLevel is a trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

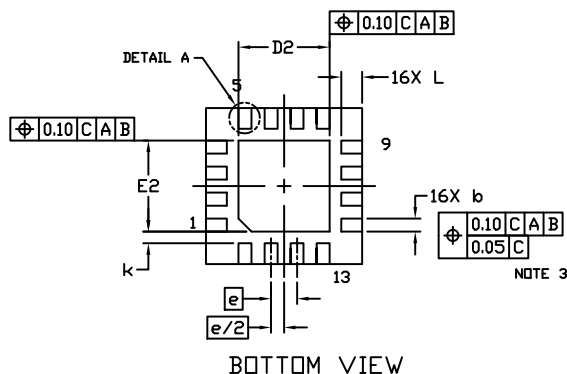
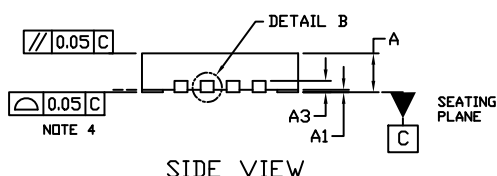
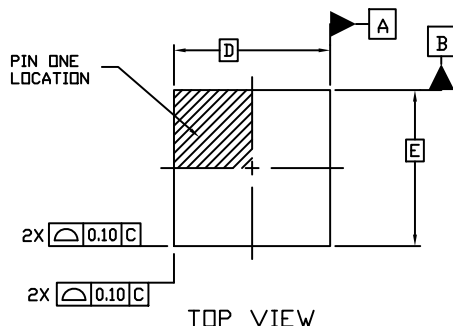
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

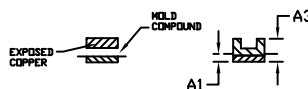
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DATE 08 OCT 2021

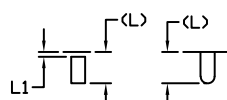


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



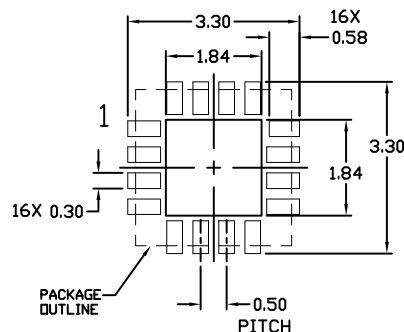
DETAIL B  
ALTERNATE  
CONSTRUCTIONS



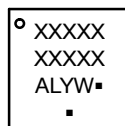
DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NDM. | MAX. |
| A   | 0.80        | 0.90 | 1.00 |
| A1  | 0.00        | 0.03 | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.18        | 0.24 | 0.30 |
| D   | 3.00 BSC    |      |      |
| D2  | 1.65        | 1.75 | 1.85 |
| E   | 3.00 BSC    |      |      |
| E2  | 1.65        | 1.75 | 1.85 |
| e   | 0.50 BSC    |      |      |
| k   | 0.18 TYP    |      |      |
| L   | 0.30        | 0.40 | 0.50 |
| L1  | 0.00        | 0.08 | 0.15 |

### MOUNTING FOOTPRINT



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                  |                 |                                                                                                                                                                                     |
|------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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