THS403x 100MHz, Low-Noise, High-Speed Amplifiers

1 Features

- Ultra-low 1.2nV/√Hz voltage noise
- High speed:
  - 100MHz bandwidth [G = 2 (–1), –3dB]
  - 100V/µs slew rate
- Very low distortion
  - THD = –81dBc (f = 1MHz, R_L = 150Ω)
  - THD = –96dBc (f = 1MHz, R_L = 1kΩ)
- Low 0.3mV (typical) input offset voltage
- 200mA output current drive (typical)
- Typical operation from ±4.5V to ±16V
- Offset nulling pins on the THS4031

2 Applications

- Low-noise, wide-band amplifier for industrial applications
- Voltage-controlled oscillators
- Active filters
- Video amplifiers
- Cable drivers
- Ultrasound scanner
- Vector signal transceiver (VST)
- Data acquisition (DAQ)

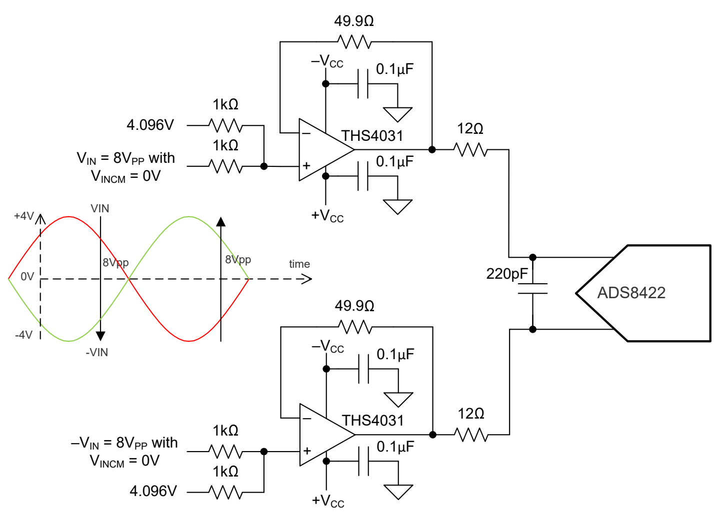
3 Description

The THS4031 and THS4032 (THS403x) are ultra-low voltage noise, high-speed voltage feedback amplifiers that are an excellent choice for applications requiring low voltage noise, including communications and imaging. The single-amplifier THS4031 and the dual-amplifier THS4032 offer very good ac performance with 100MHz bandwidth (G = 2), 100V/µs slew rate, and 70ns settling time (0.1%). The THS403x are unity-gain stable with 120MHz bandwidth. These amplifiers have a high drive capability of 200mA and draw only 7.5mA supply current per channel. With –96dBc of total harmonic distortion (THD) at f = 1MHz and a very low noise of 1.2nV/√Hz, the THS403x are designed for applications requiring low distortion and low noise such as buffering analog-to-digital converters.

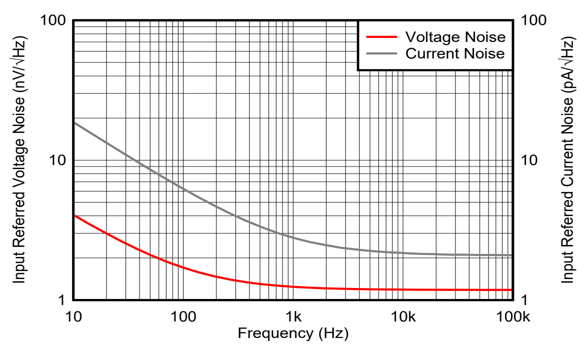
Package Information

PART NUMBER	AMPLIFIERS	PACKAGE(1)	PACKAGE SIZE(2)
THS4031	One	D (SOIC, 8)	4.9mm × 6mm
		DGN (HVSSOP, 8)	3.0mm × 4.9mm
THS4032	Two	D (SOIC, 8)	4.9mm × 6mm
		DGN (HVSSOP, 8)	3.0mm × 4.9mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



High-Performance, Low-Noise Driver for 16-Bit SAR ADCs



Voltage and Current Noise vs Frequency

Table of Contents

4 Pin Configuration and Functions

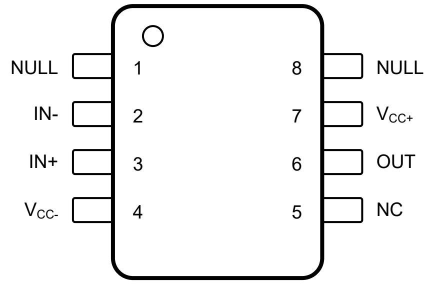


Figure 4-1. THS4031: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

Table 4-1. Pin Functions: THS4031

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN–	2	Input	Inverting input
IN+	3	Input	Non-inverting input
NC	5	—	No connection
NULL	1, 8	Input	Voltage offset adjust
OUT	6	Output	Output of amplifier
$V_{CC–}$	4	—	Negative power supply
V_{CC+}	7	—	Positive power supply

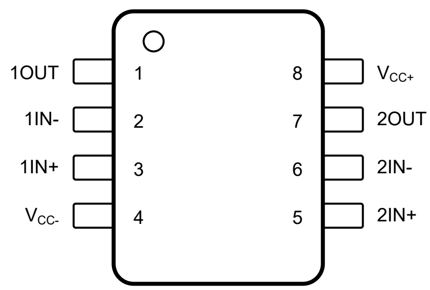


Figure 4-2. THS4032: D Package, 8-Pin SOIC, or DGN Package, 8-pin HVSSOP (Top View)

Table 4-2. Pin Functions: THS4032

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN–	2	Input	Channel 1 inverting input
1IN+	3	Input	Channel 1 non-inverting input
1OUT	1	Output	Channel 1 output
2IN–	6	Input	Channel 2 inverting input
2IN+	5	Input	Channel 2 non-inverting input
2OUT	7	Output	Channel 2 output
$V_{CC–}$	4	—	Negative power supply
V_{CC+}	8	—	Positive power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC-} to V_{CC+}	Supply voltage			33	V
V_I	Input voltage			$\pm V_{CC}$	V
I_O	Output current[2]			240	mA
V_{IO}	Differential input voltage			±1.5	V
I_{IN}	Continuous input current			10	mA
T_A	Operating free-air temperature	C-suffix	0	70	°C
		I-suffix	–40	85	
T_J	Junction temperature	Any condition		150	°C
		Maximum junction temperature, continuous operation, long term reliability[3]		130	
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) When continuously operating at any output current, do not exceed the maximum junction temperature. Keep the output current less than the absolute maximum rating regardless of time interval.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation greater than this temperature can result in reduced reliability, lifetime of the device, or both.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±1000	V
		Charged device model (CDM), per JEDEC specification JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Dual-supply	±4.5	±15	±16	V
		Single-supply	9	30	32	
T_A	Operating free-air temperature	C-suffix	0	25	70	°C
		I-suffix	–40	25	85	

5.4 Thermal Information - THS4031

THERMAL METRIC[(1)]		THS4031 D (SOIC) 8 PINS	THS4031 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124.5	60.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.0	87.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	33	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.6	7.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.3	32.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information - THS4032

THERMAL METRIC[(1)]		THS4032 D (SOIC) 8 PINS	THS4032 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.2	56.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.8	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.4	37.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	18.2	2.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61	37.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics - THS4031, R_L = 150Ω

at T_A = 25°C, V_{CC} = ±15V, and R_L = 150Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3dB)	Gain = –1V/V or 2V/V	V_{CC} = ±15V		100		MHz
			V_{CC} = ±5V		90		
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	V_{CC} = ±15V		9		MHz
			V_{CC} = ±5V		9		
SR	Slew rate[(1)]	Gain = –1V/V	V_{CC} = ±15V, 20V step		100		V/µs
			V_{CC} = ±5V, 5V step		80		
t_S	Settling time	To 0.1%, gain = –1V/V	V_{CC} = ±15V, 5V step		70		ns
			V_{CC} = ±5V, 2.5V step		55		
		To 0.01%, gain = –1V/V	V_{CC} = ±15V, 5V step		90		
			V_{CC} = ±5V, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	Gain = 2V/V, V_{CC} = ±5V or ±15V, f = 1MHz $V_{O(pp)}$ = 2V			–81		dBc
V_n	Input voltage noise	V_{CC} = ±5V or ±15V, f > 10kHz			1.2		nV/√Hz
I_n	Input current noise	V_{CC} = ±5V or ±15V, f > 10kHz			2.3		pA/√Hz
	Differential gain error	Gain = 2V/V, 40 IRE modulation, NTSC and PAL, ±100 IRE ramp	V_{CC} = ±15V		0.015%		
			V_{CC} = ±5V		0.02%		
	Differential phase error		V_{CC} = ±15V		0.025		°
			V_{CC} = ±5V		0.03		
DC PERFORMANCE							
	Open-loop gain	V_{CC} = ±15V, V_O = ±10V	T_A = 25°C	93	100		dB
			T_A = full range	92			
		V_{CC} = ±5V, V_O = ±2.5V	T_A = 25°C	90	98		
			T_A = full range	89			
V_{OS}	Input offset voltage	V_{CC} = ±5V or ±15V	T_A = 25°C		0.3	2	mV
			T_A = full range			3	
	Offset voltage drift	V_{CC} = ±5V or ±15V, T_A = full range			2		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5V or ±15V	T_A = 25°C		9	20	µA
			T_A = full range			33	
I_{OS}	Input offset current	V_{CC} = ±5V or ±15V	T_A = 25°C		30	250	nA
			T_A = full range			400	
	Input offset current	V_{CC} = ±5V or ±15V, T_A = full range			0.2		nA/°C
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15V		±13.5	±14.3		V
		V_{CC} = ±5V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15V, V_{ICR} = ±12V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±5V, V_{ICR} = ±2.5V	T_A = 25°C	90	100		
			T_A = full range	85			
R_i	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15V, R_L = 250Ω		±12	±12.9		V
		V_{CC} = ±5V		±3	±3.5		
I_O	Output current[(2)]	R_L = 10Ω	V_{CC} = ±15V	60	200		mA
			V_{CC} = ±5V	50	160		
R_O	Output resistance	Open loop			5		Ω

5.6 Electrical Characteristics - THS4031, R_L = 150Ω (continued)

at T_A = 25°C, V_{CC} = ±15V, and R_L = 150Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15V	T_A = 25°C		7.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5V	T_A = 25°C		6.5	9	
			T_A = full range			10.5	
PSRR	Power-supply rejection ratio	V_{CC} = ±5V or ±15V	T_A = 25°C	85	95		dB
			T_A = full range	80			

(1) Slew rate is measured from an output level range of 25% to 75%.
(2) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also *Section 5.1*.

5.7 Electrical Characteristics - THS4031, R_L = 1kΩ

at T_A = full range, V_{CC} = ±15V, and R_L = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
	Unity gain bandwidth	V_{CC} = ±15V, closed loop		100[(1)]	120		MHz
BW	Small-signal bandwidth (–3dB)	Gain = –1V/V or 2V/V	V_{CC} = ±15V		100		MHz
			V_{CC} = ±5V		90		
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	V_{CC} = ±15V		9		MHz
			V_{CC} = ±5V		9		
	Full power bandwidth[(2)]	V_{CC} = ±15V, $V_{O(pp)}$ = 20V			1.6		MHz
		V_{CC} = ±5V, $V_{O(pp)}$ = 5V			5.1		
SR	Slew rate			80[(1)]	100		V/µs
t_S	Settling time	To 0.1%, gain = –1V/V	V_{CC} = ±15V, 5V step		70		ns
			V_{CC} = ±5V, 2.5V step		55		
		To 0.01%, gain = –1V/V	V_{CC} = ±15V, 5V step		90		
			V_{CC} = ±5V, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	Gain =2V/V, V_{CC} = ±5V or ±15V, f = 1MHz $V_{O(pp)}$ = 2V			–96		dBc
DC PERFORMANCE							
	Open-loop gain	V_{CC} = ±15V, V_O = ±10V	T_A = 25°C	93	100		dB
			T_A = full range	92			
		V_{CC} = ±5V, V_O = ±2.5V	T_A = 25°C	92	98		
			T_A = full range	91			
V_{OS}	Input offset voltage	V_{CC} = ±5V or ±15V	T_A = 25°C		0.3	2	mV
			T_A = full range			3	
	Offset voltage drift	V_{CC} = ±5V or ±15V, T_A = full range			2		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5V or ±15V	T_A = 25°C		9	20	µA
			T_A = full range			33	
I_{OS}	Input offset current	V_{CC} = ±5V or ±15V	T_A = 25°C		30	250	µA
			T_A = full range			400	
	Input offset current drift	V_{CC} = ±5V or ±15V, T_A = full range			0.2		nA/°C

5.7 Electrical Characteristics - THS4031, R_L = 1kΩ (continued)

at T_A = full range, V_{CC} = ±15V, and R_L = 1kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15V		±13.5	±14.3		V
		V_{CC} = ±5V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15V, V_{ICR} = ±12V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±5V, V_{ICR} = ±2.5V	T_A = 25°C	90	100		
			T_A = full range	85			
R_i	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15V		±13	±13.6		V
		V_{CC} = ±5V		±3.4	±3.8		
R_O	Output resistance	Open loop			5		Ω
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15V	T_A = 25°C		7.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5V	T_A = 25°C		6.5	9	
			T_A = full range			10	
PSRR	Power-supply rejection ratio	V_{CC} = ±5V or ±15V	T_A = 25°C	85	95		dB
			T_A = full range	80			

(1) This minimum value is not tested.
(2) Full power bandwidth = slew rate / [$\pi V_{O(P-P)}$].

5.8 Electrical Characteristics - THS4032, R_L = 150Ω

at T_A = 25°C, V_{CC} = ±15V, and R_L = 150Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
BW	Small-signal bandwidth (–3 dB)	Gain = –1V/V or 2V/V	V_{CC} = ±15V		100		MHz
			V_{CC} = ±5V		90		
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	V_{CC} = ±15V		50		MHz
			V_{CC} = ±5V		45		
SR	Slew rate[(1)]	Gain = –1V/V	V_{CC} = ±15V, 20V step		100		V/μs
			V_{CC} = ±5V, 5V step		80		
t_S	Settling time	To 0.1%, Gain = –1V/V	V_{CC} = ±15V, 5V step		60		ns
			V_{CC} = ±5V, 2.5V step		45		
		To 0.01%, Gain = –1V/V	V_{CC} = ±15V, 5V step		90		
			V_{CC} = ±5V, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	Gain = 2V/V, V_{CC} = ±5V or ±15V, f = 1MHz $V_{O(pp)}$ = 2V			–72		dBc
V_n	Input voltage noise	V_{CC} = ±5V or ±15V, f > 10kHz			1.6		nV/√Hz
I_n	Input current noise	V_{CC} = ±5V or ±15V, f > 10kHz			1.2		pA/√Hz
	Differential gain error	Gain = 2V/V, 40 IRE modulation, NTSC and PAL, ±100 IRE ramp	V_{CC} = ±15V		0.015%		
			V_{CC} = ±5V		0.02%		
	Differential phase error		V_{CC} = ±15V		0.025		°
			V_{CC} = ±5V		0.03		
	Channel-to-channel crosstalk (THS4032 only)	V_{CC} = ±5V or ±15V, f = 1MHz			–61		dBc
DC PERFORMANCE							
V_{OS}	Input offset voltage	V_{CC} = ±5V or ±15V	T_A = 25°C		0.5	2	mV
			T_A = full range			3	
I_{OS}	Input offset current	V_{CC} = ±5V or ±15V	T_A = 25°C		30	250	nA
			T_A = full range			400	
	Offset voltage drift	V_{CC} = ±5V or ±15V, T_A = full range			2		μV/°C
	Input offset current drift	V_{CC} = ±5V or ±15V, T_A = full range			0.2		nA/°C
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15V		±13.5	±14		V
		V_{CC} = ±5V		±3.8	±4		
CMRR	Common-mode rejection ratio	V_{CC} = ±15V, V_{ICR} = ±12V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±5 V, V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
			T_A = full range	85			
R_i	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15V, R_L = 250Ω		±12	±12.9		V
		V_{CC} = ±5V		±3	±3.5		
I_O	Output current[(2)]	R_L = 20Ω	V_{CC} = ±15V	60	90		mA
			V_{CC} = ±5V	50	70		
I_{SC}	Short-circuit current[(2)]	V_{CC} = ±15V			150		mA
R_O	Output resistance	Open loop			13		Ω

5.8 Electrical Characteristics - THS4032, R_L = 150Ω (continued)

at T_A = 25°C, V_{CC} = ±15V, and R_L = 150Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15V	T_A = 25°C		8.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5V	T_A = 25°C		7.5	9	
			T_A = full range			10.5	
PSRR	Power-supply rejection ratio	V_{CC} = ±5V or ±15V	T_A = 25°C	85	95		dB
			T_A = full range	80			

(1) Slew rate is measured from an output level range of 25% to 75%.
(2) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also Section 5.1.

5.9 Electrical Characteristics - THS4032, R_L = 1kΩ

at T_A = full range, V_{CC} = ±15 V, and R_L = 1 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE							
	Unity gain bandwidth	V_{CC} = ±15V, closed loop		100[1]	120		MHz
BW	Small-signal bandwidth (–3dB)	Gain = –12V/V or 2V/V	V_{CC} = ±15V		100		MHz
			V_{CC} = ±5V		90		
	Bandwidth for 0.1dB flatness	Gain = –1V/V or 2V/V	V_{CC} = ±15V		50		MHz
			V_{CC} = ±5V		45		
	Full power bandwidth[2]	V_{CC} = ±15V, $V_{O(pp)}$ = 20V			2.3		MHz
		V_{CC} = ±5V, $V_{O(pp)}$ = 5V			7.1		
SR	Slew rate	V_{CC} = ±15V		80[1]	100		V/µs
t_S	Settling time	To 0.1%, Gain = –1V/V	V_{CC} = ±15V, 5V step		60		ns
			V_{CC} = ±5V, 2.5V step		45		
		To 0.01%,Gain = –1V/V	V_{CC} = ±15V, 5V step		90		
			V_{CC} = ±5V, 2.5V step		80		
NOISE AND DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V_{CC} = ±5 V or ±15 V, f = 1 MHz, Gain = 2V/V, $V_{O(pp)}$ = 2 V, T_A = 25°C			–96		dBc
DC PERFORMANCE							
	Open loop gain	V_{CC} = ±15V, V_O = ±10V	T_A = 25°C	93	98		dB
			T_A = full range	92			
		V_{CC} = ±5V, V_O = ±2.5V	T_A = 25°C	92	95		
			T_A = full range	91			
V_{OS}	Input offset voltage	V_{CC} = ±5V or ±15V	T_A = 25°C		0.5	2	mV
			T_A = full range			3	
I_{IB}	Input bias current	V_{CC} = ±5V or ±15V	T_A = 25°C		3	6	µA
			T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5V or ±15V	T_A = 25°C		30	250	nA
			T_A = full range			400	
	Input offset current drift	V_{CC} = ±5V or ±15V,T_A = full range			0.2		nA/°C
	Offset voltage drift	V_{CC} = ±5V or ±15V, T_A = full range			2		µV/°C

5.9 Electrical Characteristics - THS4032, R_L = 1kΩ (continued)

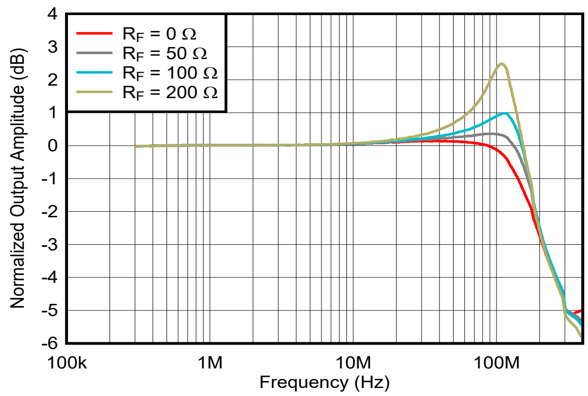
at T_A = full range, V_{CC} = ±15 V, and R_L = 1 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15V		±13.5	±14.3		V
		V_{CC} = ±5V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15V, V_{ICR} = ±12V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±5V, V_{ICR} = ±2.5V	T_A = 25°C	90	100		
			T_A = full range	85			
R_i	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15V		±13	±13.6		V
		V_{CC} = ±5V		±3.4	±3.8		V
I_0	Output current(2)	R_L = 20Ω	V_{CC} = ±15V	60	90		mA
			V_{CC} = ±5V	50	70		
I_{SC}	Short-circuit current(3)	V_{CC} = ±15V			150		mA
R_O	Output resistance	Open loop			13		Ω
POWER SUPPLY							
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15V	T_A = 25°C		8.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5V	T_A = 25°C		7.5	9	
			T_A = full range			10	
PSRR	Power-supply rejection ratio	V_{CC} = ±5V or ±15V	T_A = 25°C	85	95		dB
			T_A = full range	80			

(1) This minimum value is not tested.
(2) Full power bandwidth = slew rate / [$\sqrt{2}\,\pi V_{OC(Peak)}$].
(3) Keep junction temperature less than the absolute maximum rating when the output is heavily loaded or shorted; see also Section 5.1.

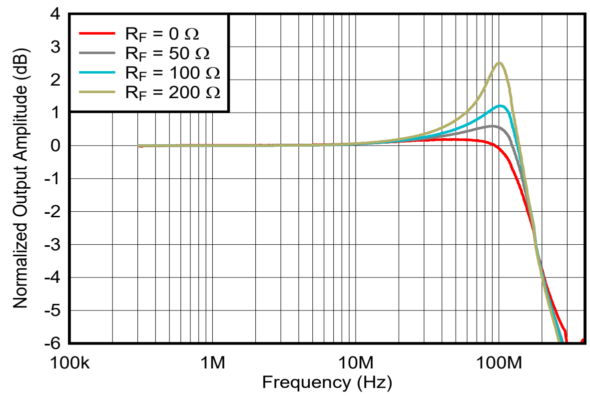
5.10 Typical Characteristics - THS4031

at T_A = 25°C, V_{CC} = ± 15 V, gain = +1 V/V, R_L = 150 Ω, and R_F = 300 Ω (unless otherwise noted)



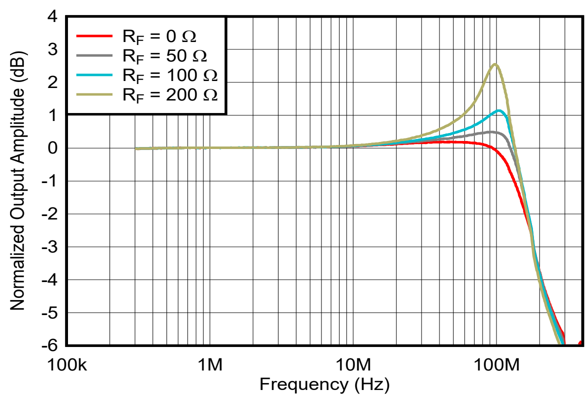
V_{CC} = ±15 V, R_L = 150 Ω, V_{OUT} = 200 mV_{PP}

Figure 5-1. Frequency Response vs Feedback Resistance



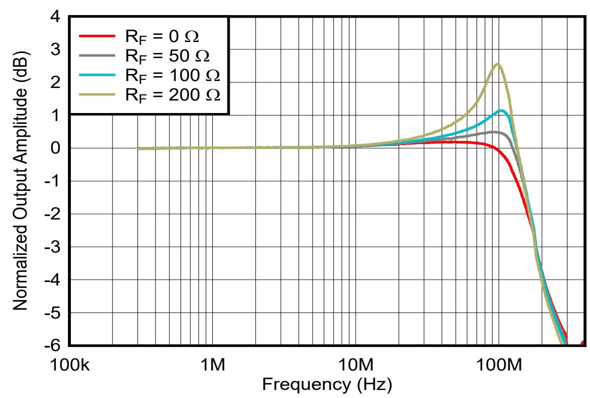
V_{CC} = ±15 V, R_L = 1 kΩ, V_{OUT} = 200 mV_{PP}

Figure 5-2. Frequency Response vs Feedback Resistance



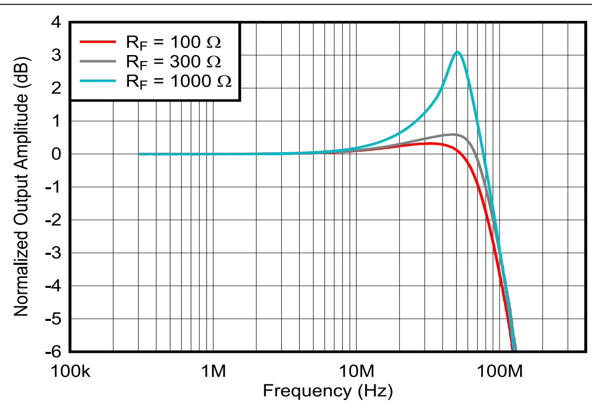
V_{CC} = ±5 V, R_L = 150 Ω, V_{OUT} = 200 mV_{PP}

Figure 5-3. Frequency Response vs Feedback Resistance



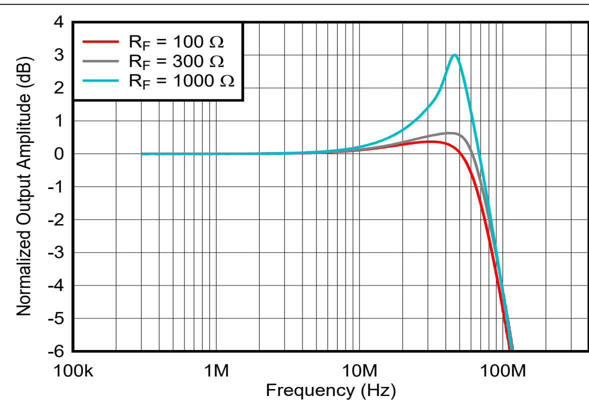
V_{CC} = ±5 V, R_L = 1 kΩ, V_{OUT} = 200 mV_{PP}

Figure 5-4. Frequency Response vs Feedback Resistance



Gain = +2 V/V, V_{OUT} = 400 mV_{PP}

Figure 5-5. Frequency Response vs Feedback Resistance

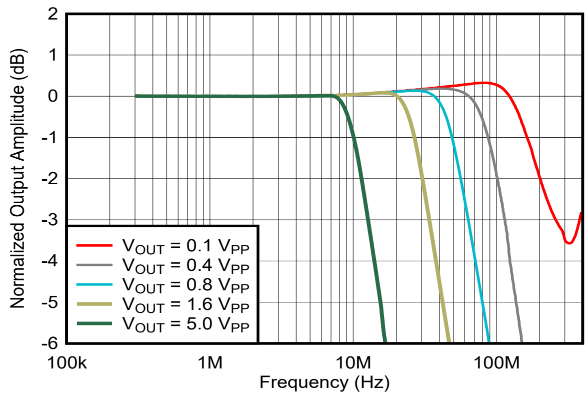


V_{CC} = ±5 V, gain = +2 V/V, V_{OUT} = 400 mV_{PP}

Figure 5-6. Frequency Response vs Feedback Resistance

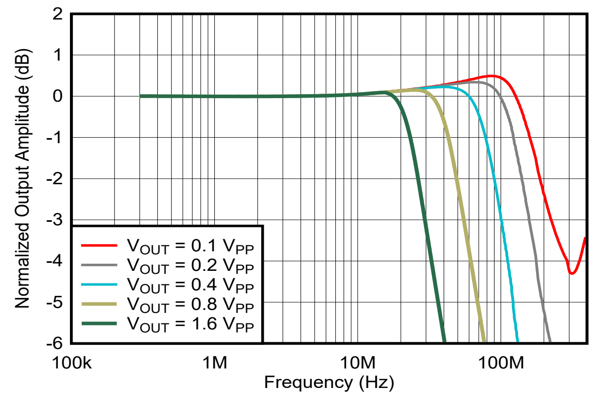
5.10 Typical Characteristics - THS4031 (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +1 V/V, R_L = 150 Ω, and R_F = 300 Ω (unless otherwise noted)



V_{CC} = ±15 V

Figure 5-7. Large-Signal Frequency Response



V_{CC} = ±5 V

Figure 5-8. Large-Signal Frequency Response

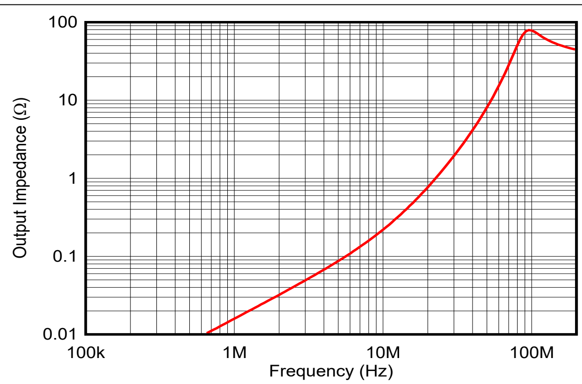


Figure 5-9. Closed-Loop Output Impedance

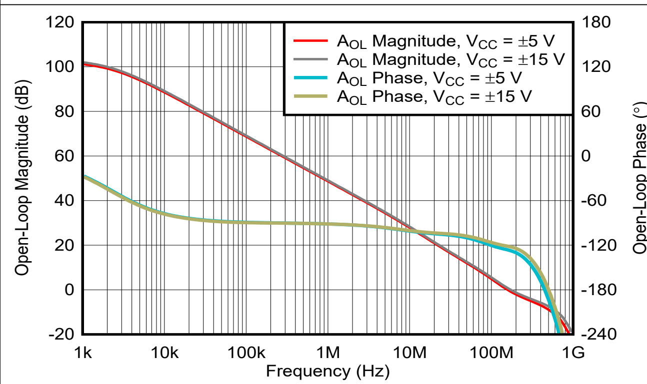


Figure 5-10. Open-Loop Gain and Phase Response

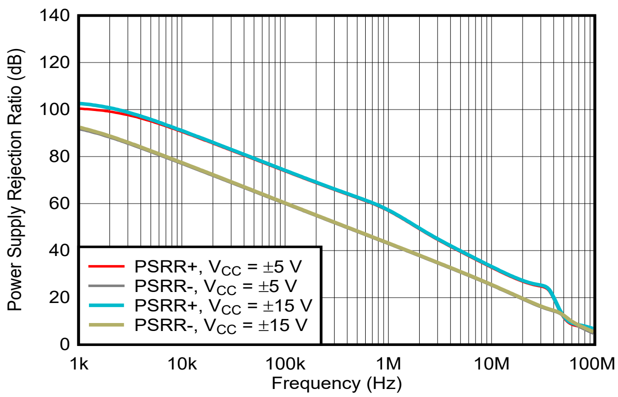


Figure 5-11. Power-Supply Rejection Ratio vs Frequency

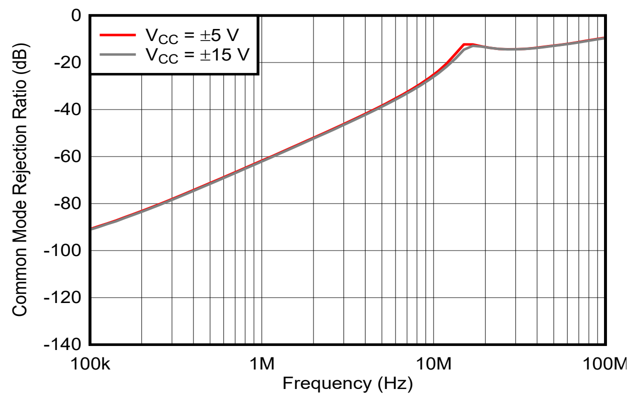


Figure 5-12. Common-Mode Rejection Ratio vs Frequency

5.10 Typical Characteristics - THS4031 (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +1 V/V, R_L = 150 Ω, and R_F = 300 Ω (unless otherwise noted)

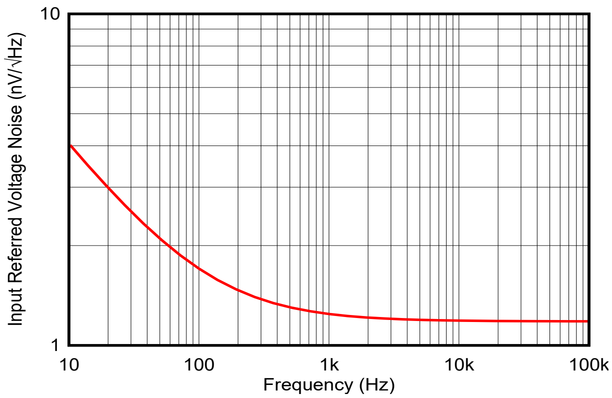


Figure 5-13. Input-Referred Voltage Noise vs Frequency

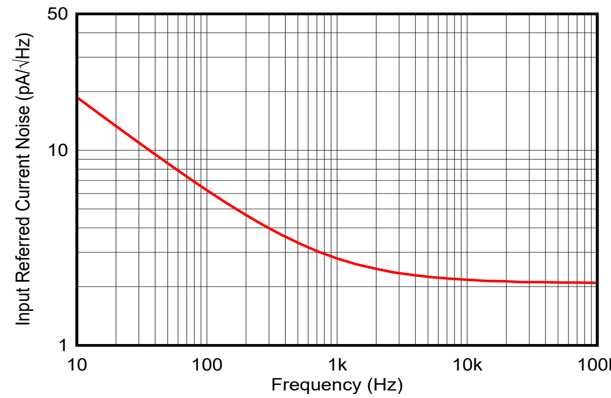
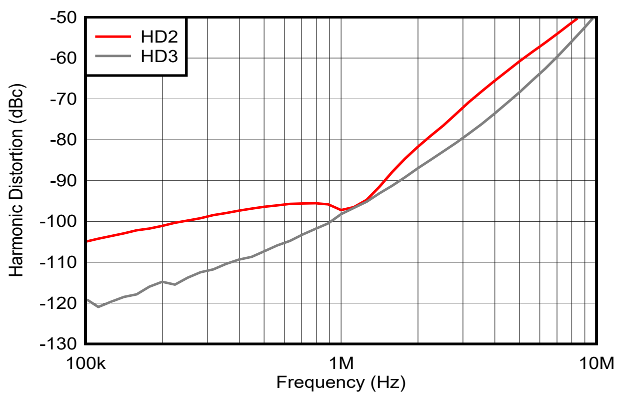
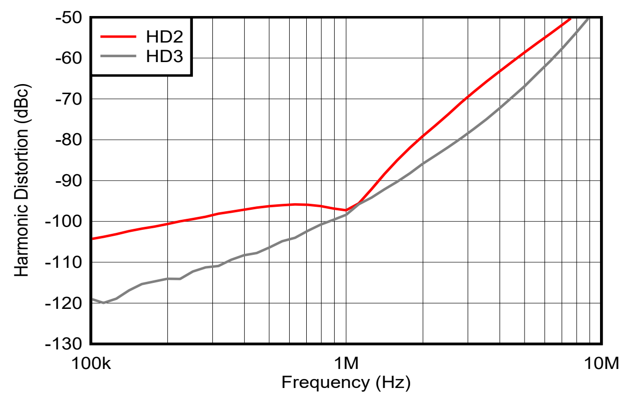


Figure 5-14. Input-Referred Current Noise vs Frequency



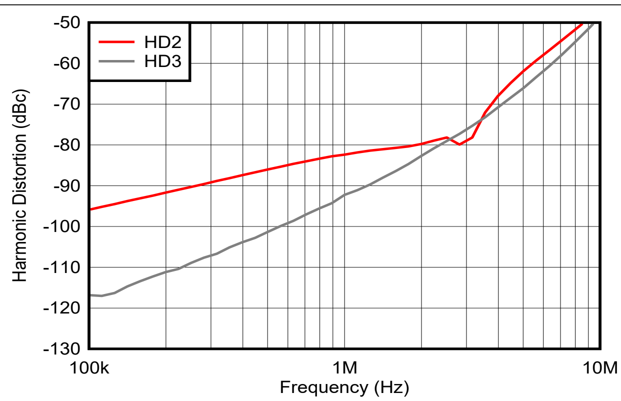
V_{CC} = ±15 V, gain = +2 V/V, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}

Figure 5-15. Harmonic Distortion vs Frequency



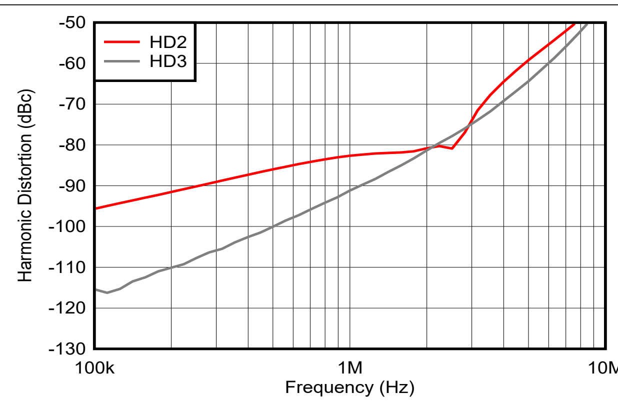
V_{CC} = ±5 V, gain = +2 V/V, R_L = 1 kΩ, V_{OUT} = 2 V_{PP}

Figure 5-16. Harmonic Distortion vs Frequency



V_{CC} = ±15 V, gain = +2 V/V, R_L = 150 Ω, V_{OUT} = 2 V_{PP}

Figure 5-17. Harmonic Distortion vs Frequency

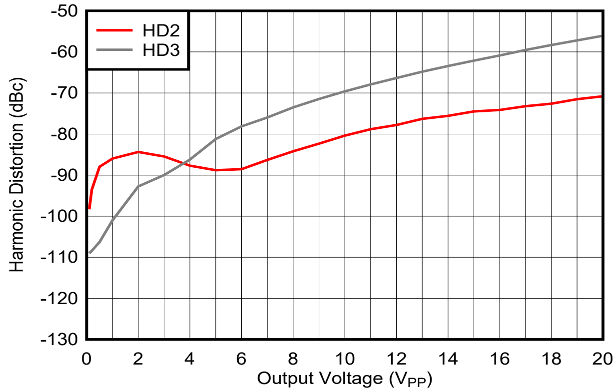


V_{CC} = ±5 V, gain = +2 V/V, R_L = 150 Ω, V_{OUT} = 2 V_{PP}

Figure 5-18. Harmonic Distortion vs Frequency

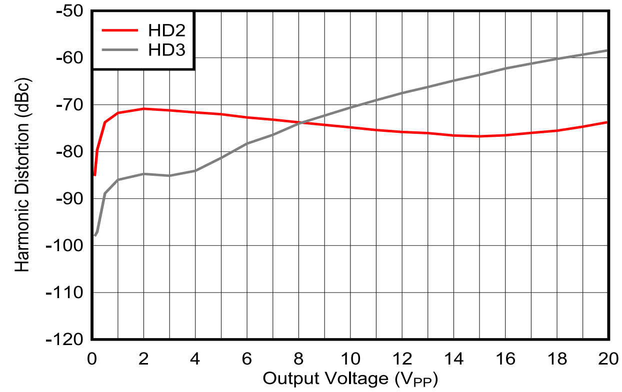
5.10 Typical Characteristics - THS4031 (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +1 V/V, R_L = 150 Ω, and R_F = 300 Ω (unless otherwise noted)



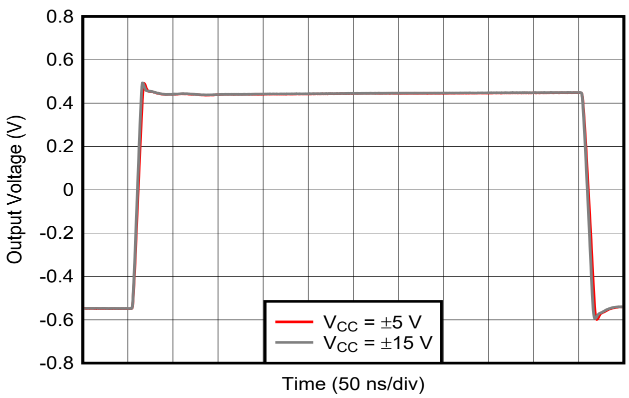
V_{CC} = ±15 V, gain = +5 V/V, R_L = 1 kΩ, f = 1 MHz

Figure 5-19. Harmonic Distortion vs Peak-to-Peak Output Voltage



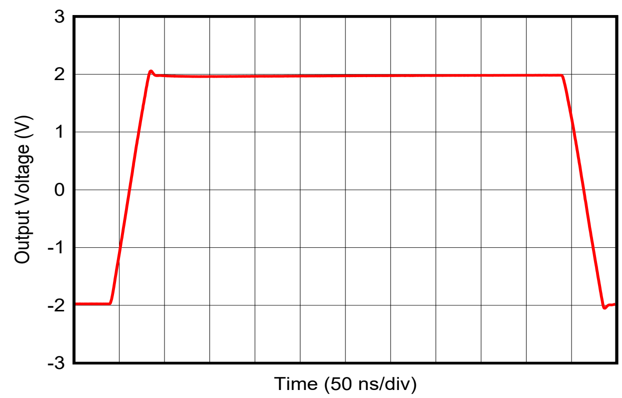
V_{CC} = ±15 V, gain = +5 V/V, R_L = 150 Ω, f = 1 MHz

Figure 5-20. Harmonic Distortion vs Peak-to-Peak Output Voltage



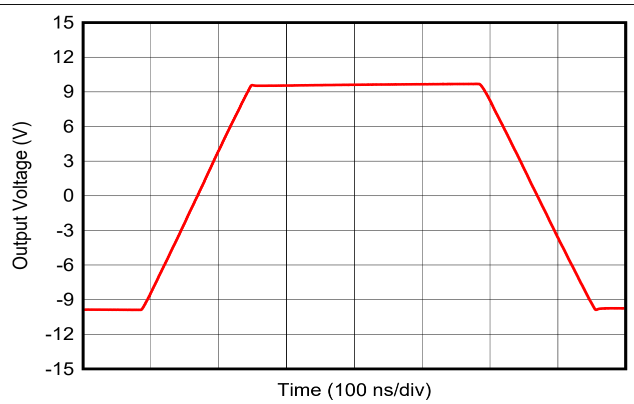
Gain = +2 V/V

Figure 5-21. 1-V Step Response



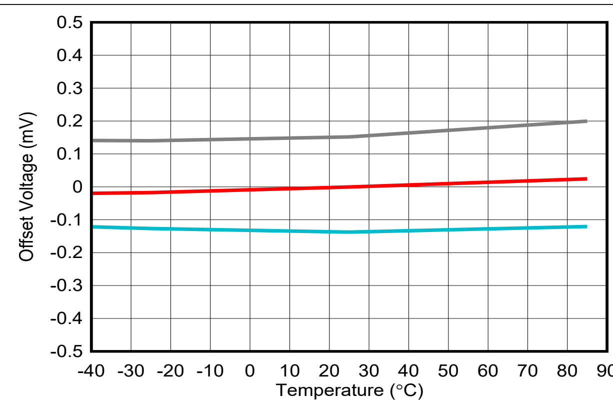
V_{CC} = ±5 V, gain =–1 V/V, R_F = 430 Ω

Figure 5-22. 4-V Step Response



Gain = +2 V/V

Figure 5-23. 20-V Step Response



3 typical units

Figure 5-24. Input Offset Voltage vs Ambient Temperature

5.10 Typical Characteristics - THS4031 (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +1 V/V, R_L = 150 Ω, and R_F = 300 Ω (unless otherwise noted)

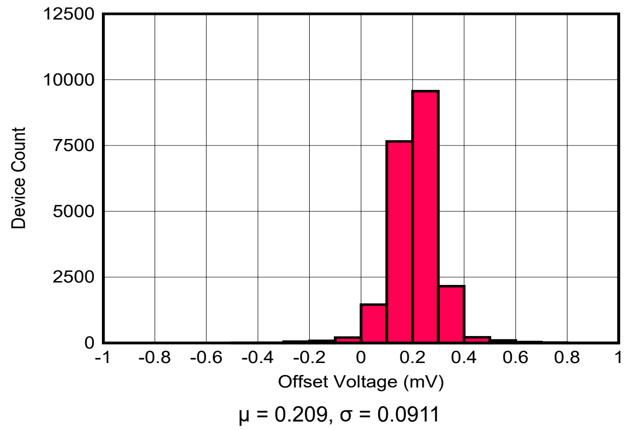


Figure 5-25. Voltage Offset Distribution

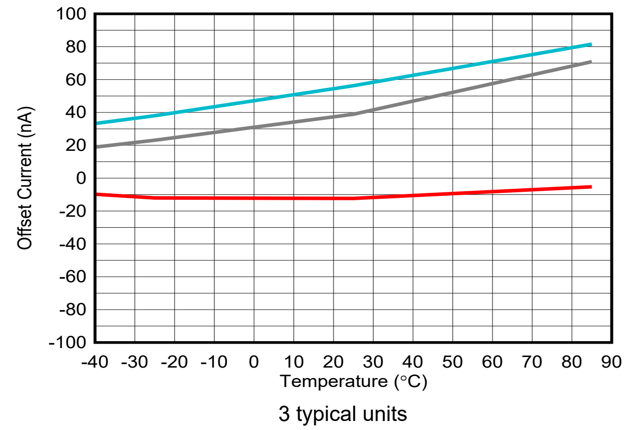


Figure 5-26. Input Offset Current vs Ambient Temperature

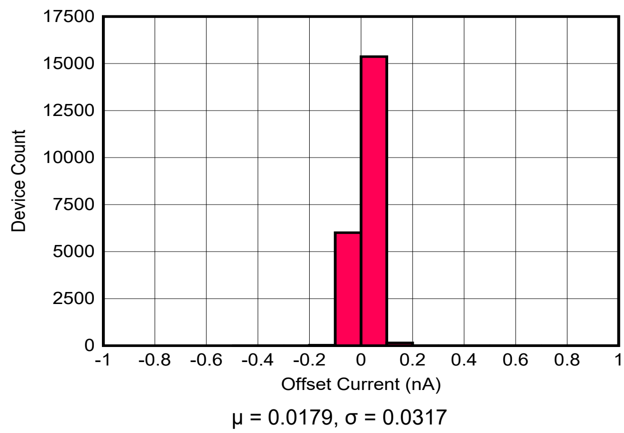


Figure 5-27. Input Offset Current vs Ambient Temperature

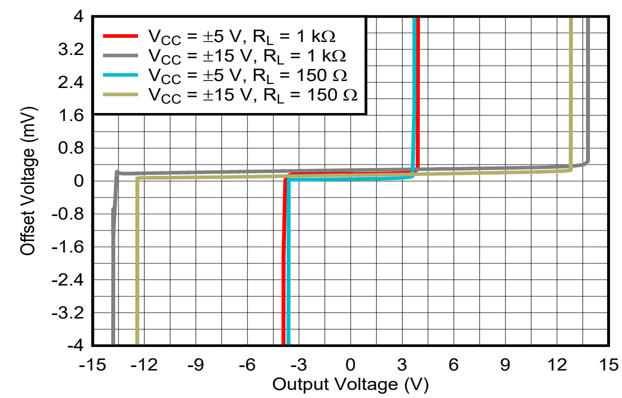


Figure 5-28. Offset Voltage vs Output Voltage

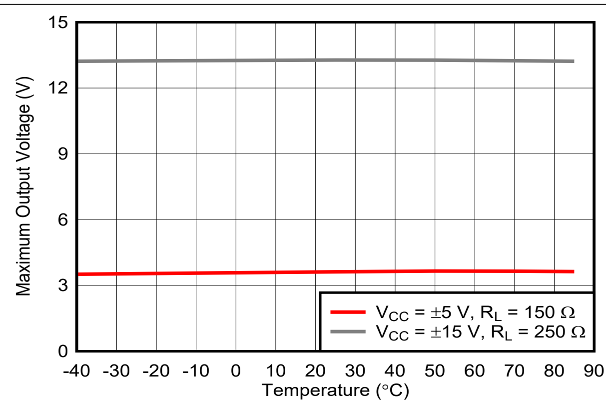


Figure 5-29. Maximum Output Voltage Swing vs Ambient Temperature

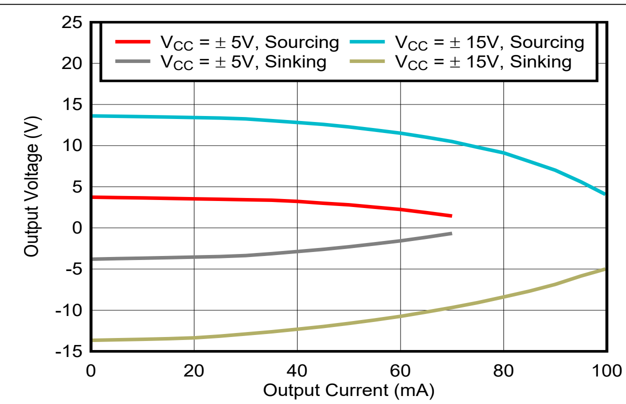


Figure 5-30. Output Swing vs Load Current

5.10 Typical Characteristics - THS4031 (continued)

at T_A = 25°C, V_{CC} = ± 15 V, gain = +1 V/V, R_L = 150 Ω, and R_F = 300 Ω (unless otherwise noted)

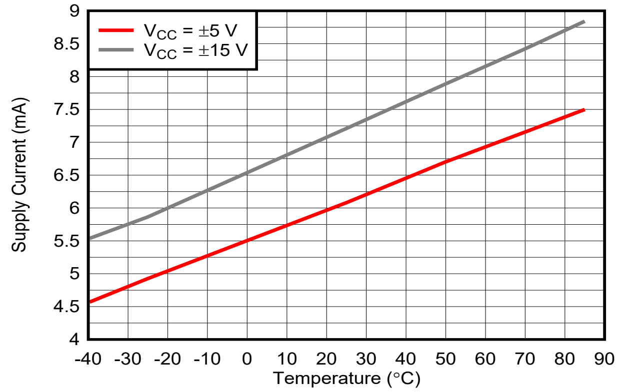


Figure 5-31. Supply Current vs Ambient Temperature

5.11 Typical Characteristics - THS4032

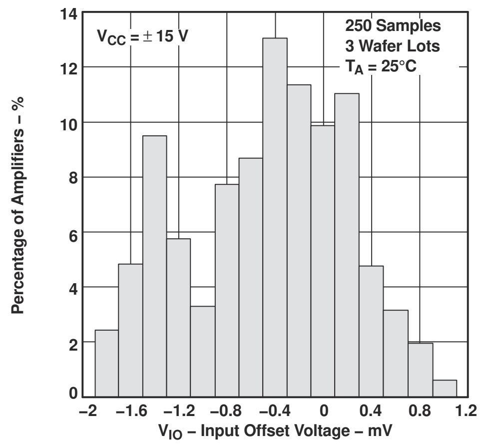


Figure 5-32. Input Offset Voltage Distribution

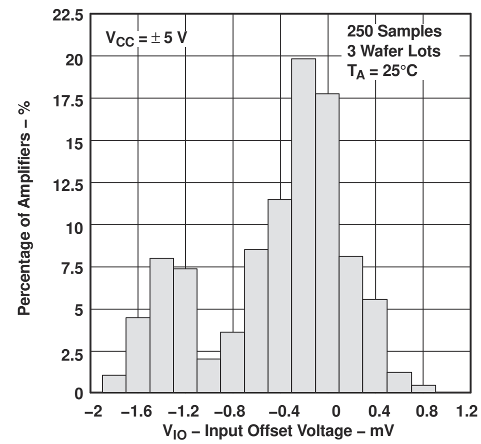


Figure 5-33. Input Offset Voltage Distribution

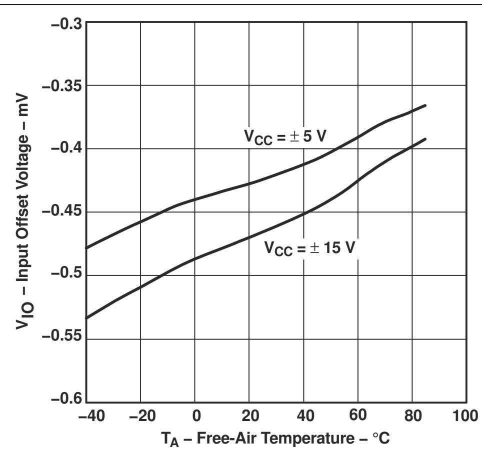


Figure 5-34. Input Offset Voltage vs Free-Air Temperature

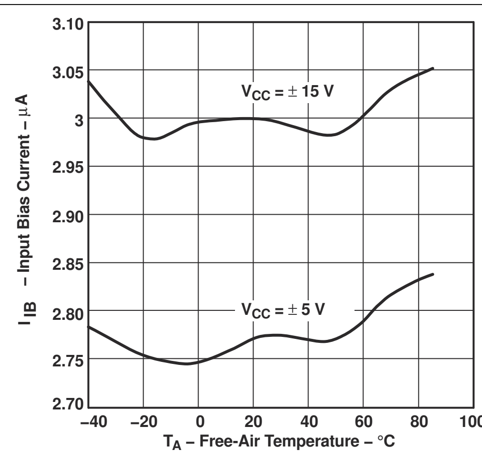


Figure 5-35. Input Bias Current vs Free-Air Temperature

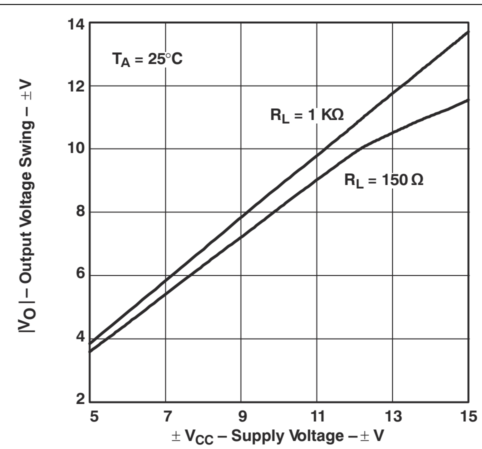


Figure 5-36. Output Voltage Swing vs Supply Voltage

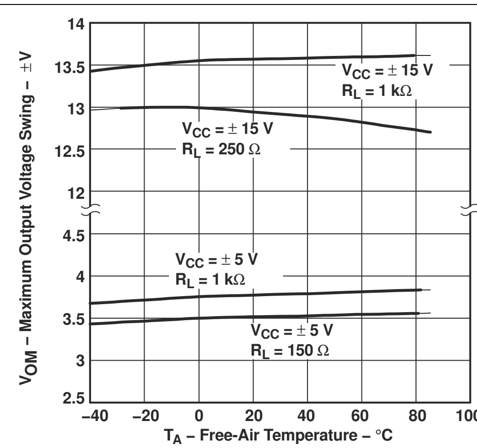


Figure 5-37. Maximum Output Voltage Swing vs Free-Air Temperature

5.11 Typical Characteristics - THS4032 (continued)

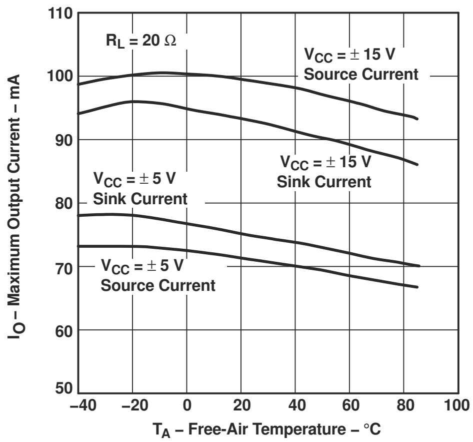


Figure 5-38. Maximum Output Current vs Free-Air Temperature

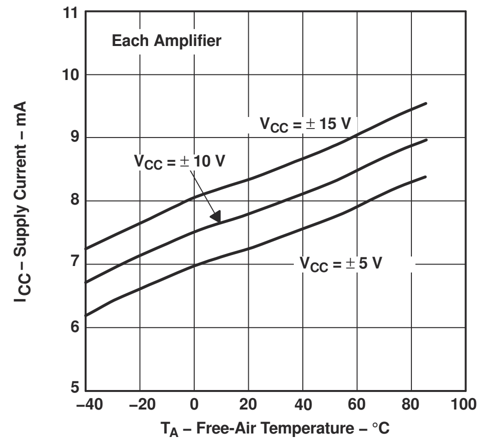


Figure 5-39. Supply Current vs Free-Air Temperature

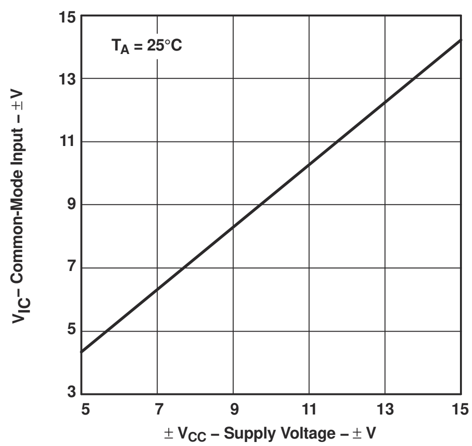


Figure 5-40. Common-Mode Input Voltage vs Supply Voltage

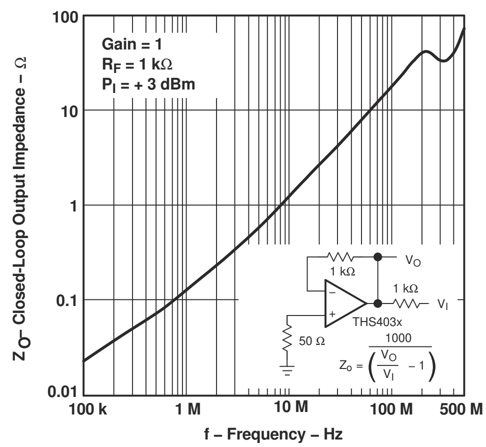


Figure 5-41. Closed-Loop Output Impedance vs Frequency

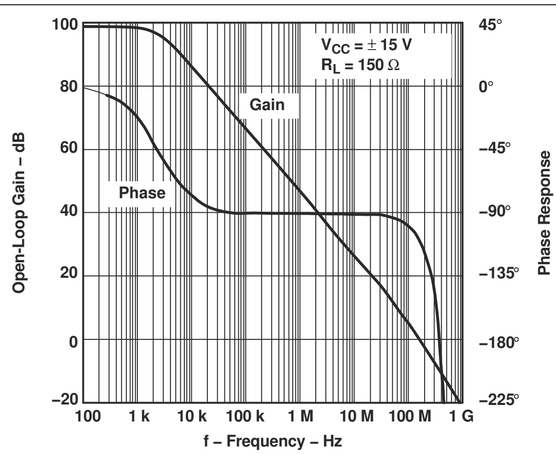


Figure 5-42. Open-Loop Gain and Phase Response

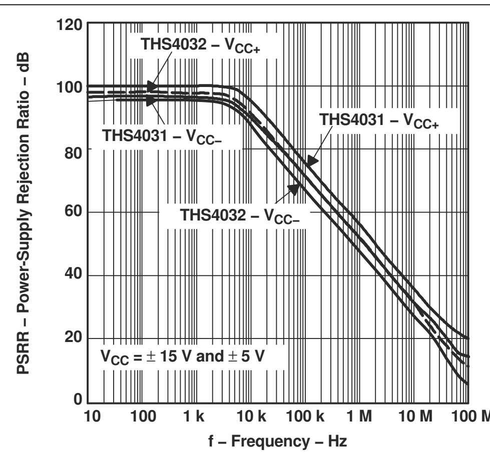


Figure 5-43. Power-Supply Rejection Ratio vs Frequency

5.11 Typical Characteristics - THS4032 (continued)

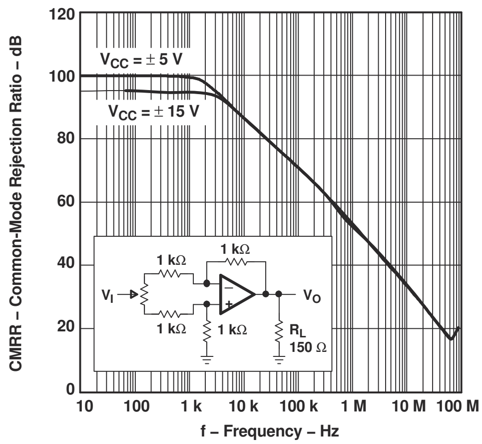


Figure 5-44. Common-Mode Rejection Ratio vs Frequency

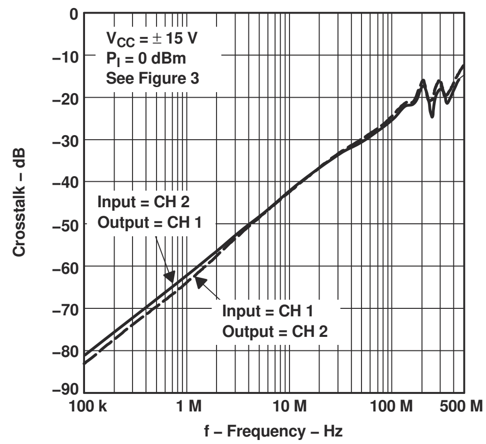


Figure 5-45. THS4032 Crosstalk vs Frequency

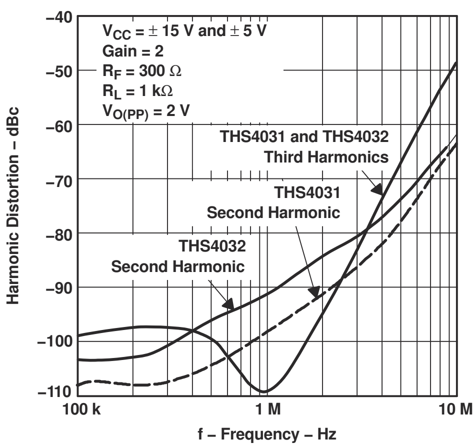


Figure 5-46. Harmonic Distortion vs Frequency

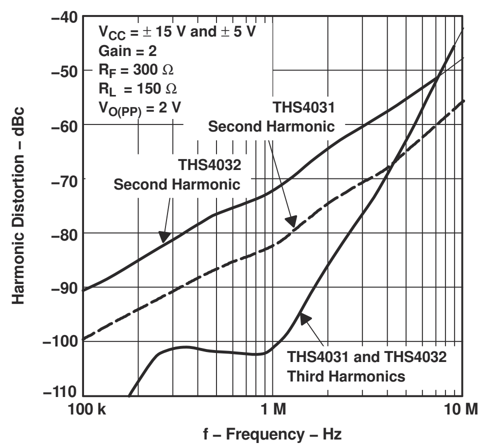


Figure 5-47. Harmonic Distortion vs Frequency

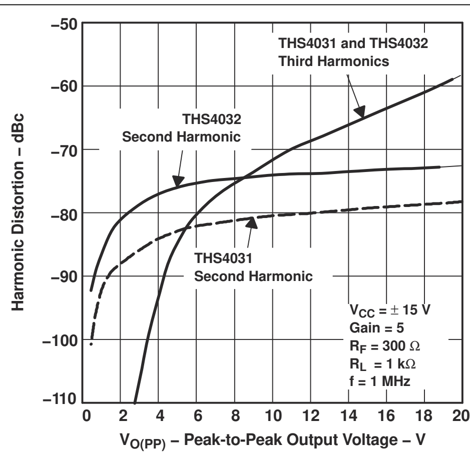


Figure 5-48. Harmonic Distortion vs Peak-to-Peak Output Voltage

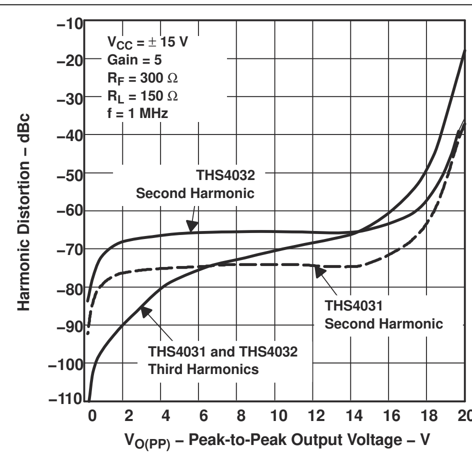


Figure 5-49. Harmonic Distortion vs Peak-to-Peak Output Voltage

5.11 Typical Characteristics - THS4032 (continued)

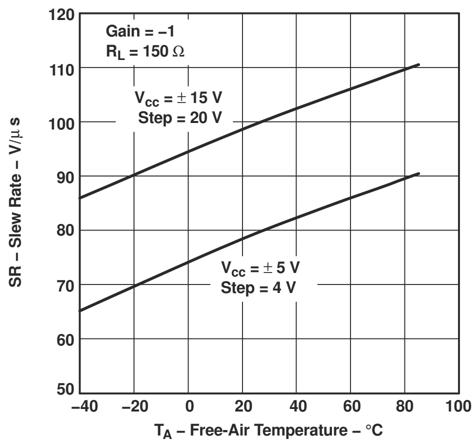


Figure 5-50. Slew Rate vs Free-Air temperature

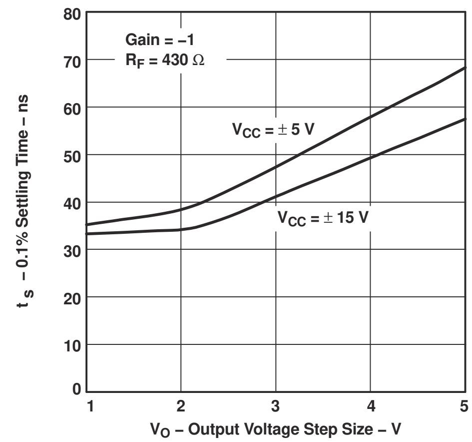


Figure 5-51. 0.1% Settling Time vs Output Voltage Step Size

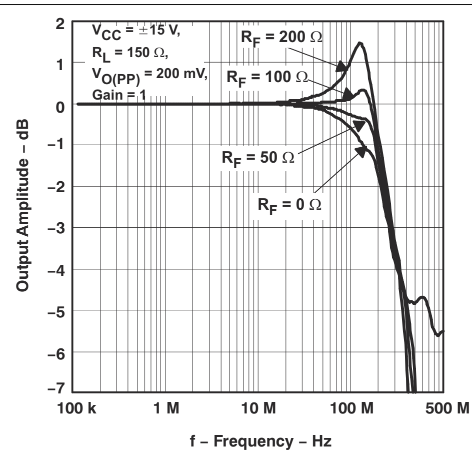


Figure 5-52. Small-Signal Frequency Response With Varying Feedback Resistance

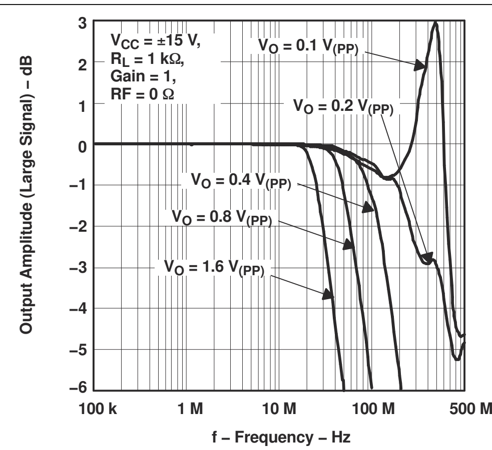


Figure 5-53. Frequency Response With Varying Output Voltage Swing

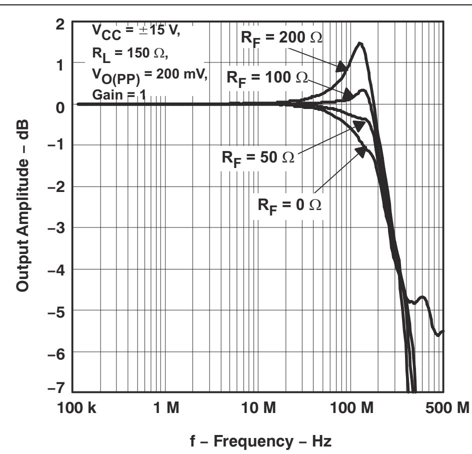


Figure 5-54. Small-Signal Frequency Response With Varying Feedback Resistance

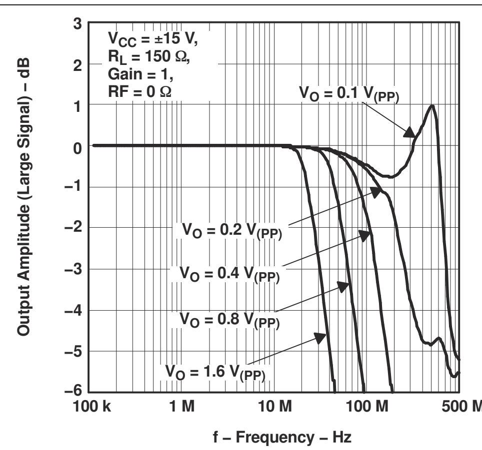


Figure 5-55. Frequency Response With Varying Output Voltage Swing

5.11 Typical Characteristics - THS4032 (continued)

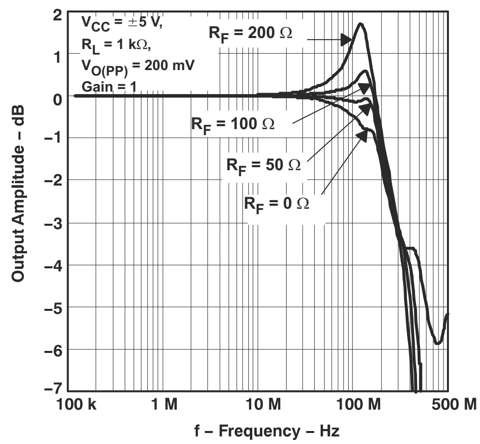


Figure 5-56. Small-Signal Frequency Response With Varying Feedback Resistance

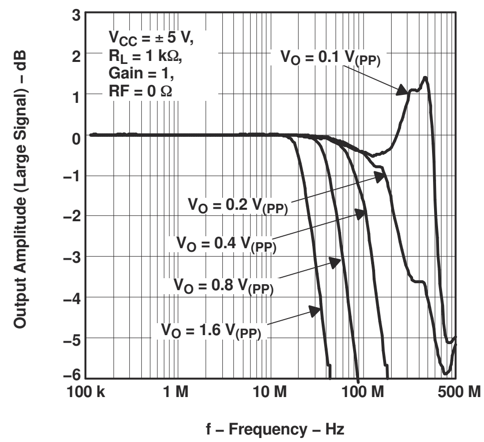


Figure 5-57. Frequency Response With Varying Output Voltage Swing

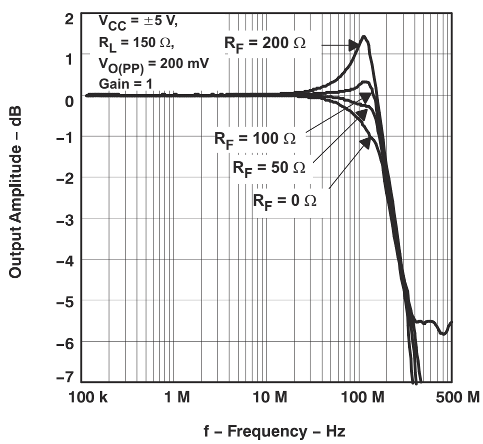


Figure 5-58. Small-Signal Frequency Response With Varying Feedback Resistance

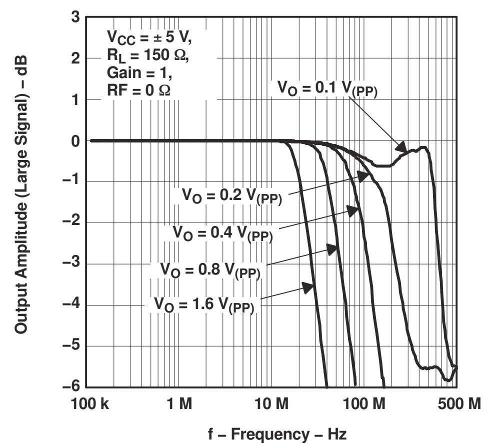


Figure 5-59. Frequency Response With Varying Output Voltage Swing

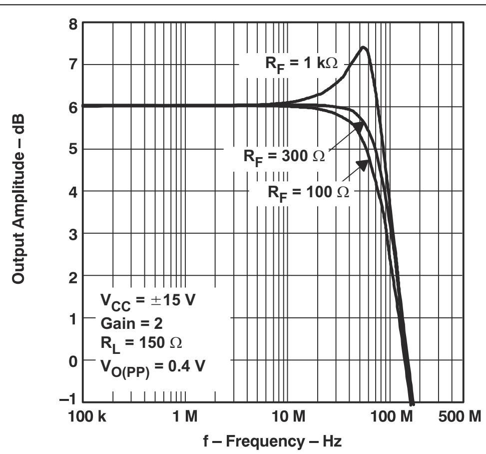


Figure 5-60. Small-Signal Frequency Response With Varying Feedback Resistance

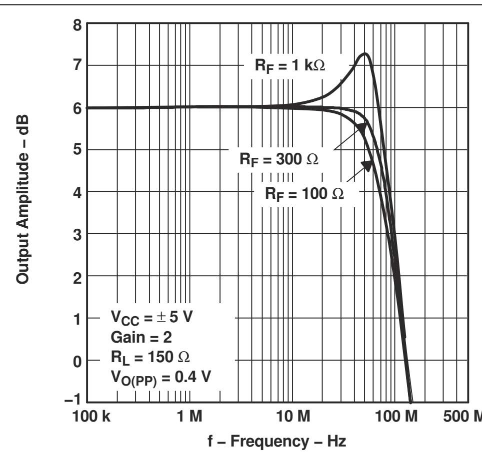


Figure 5-61. Small-Signal Frequency Response With Varying Feedback Resistance

5.11 Typical Characteristics - THS4032 (continued)

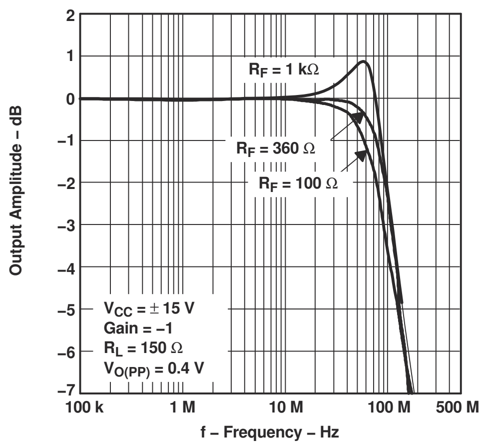


Figure 5-62. Small-Signal Frequency Response With Varying Feedback Resistance

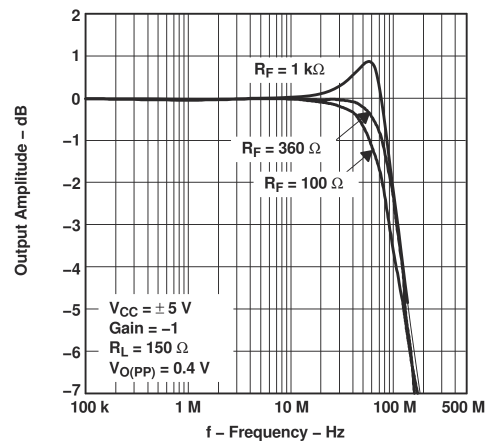


Figure 5-63. Small-Signal Frequency Response With Varying Feedback Resistance

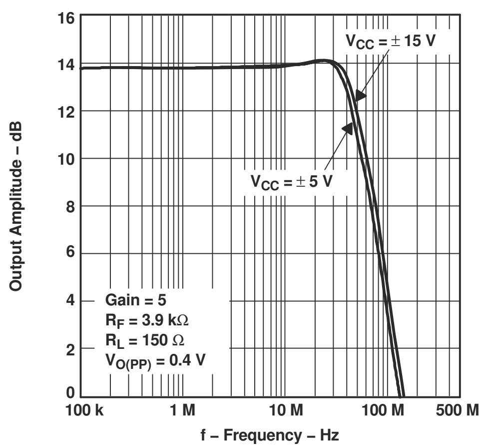


Figure 5-64. Small-Signal Frequency Response

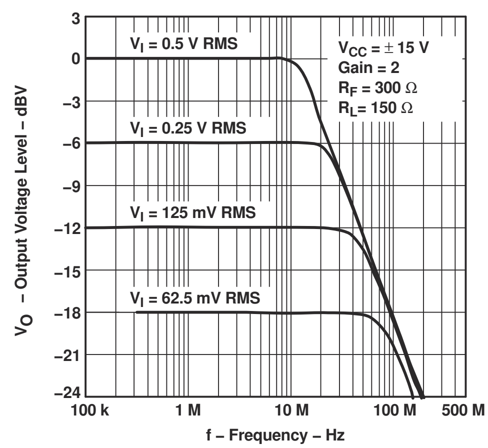


Figure 5-65. Output Amplitude vs Frequency

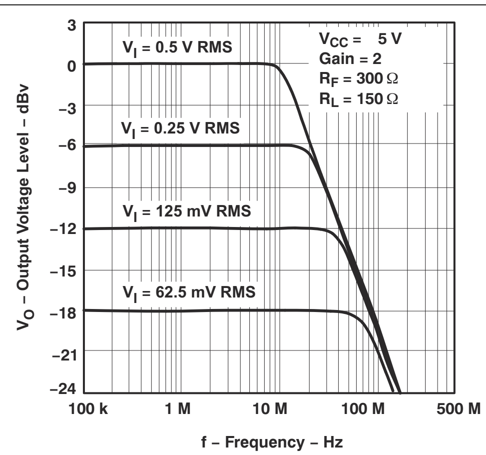


Figure 5-66. Output Amplitude vs Frequency

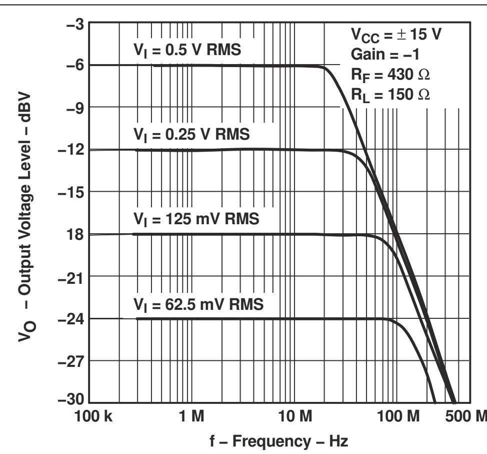


Figure 5-67. Output Amplitude vs Frequency

5.11 Typical Characteristics - THS4032 (continued)

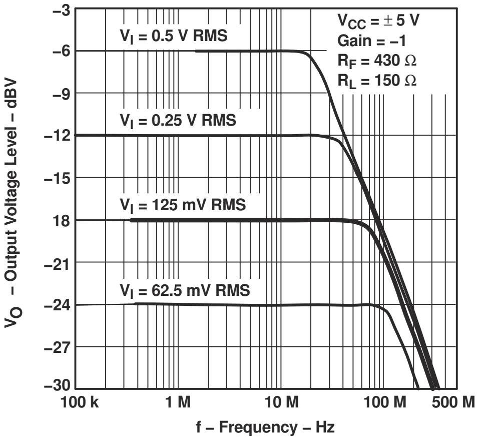


Figure 5-68. Output Amplitude vs Frequency

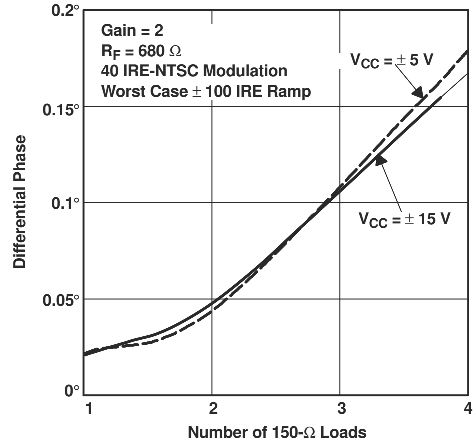


Figure 5-69. Differential Phase vs Number of 150-Ω Loads

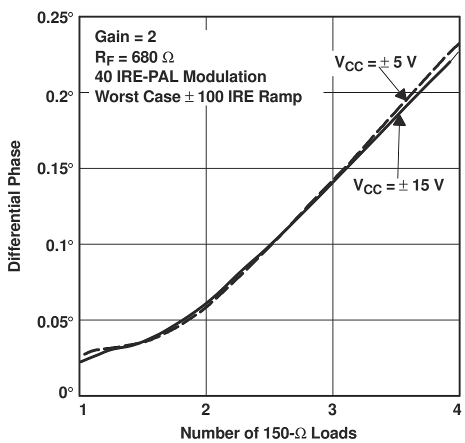


Figure 5-70. Differential Phase vs Number of 150-Ω Loads

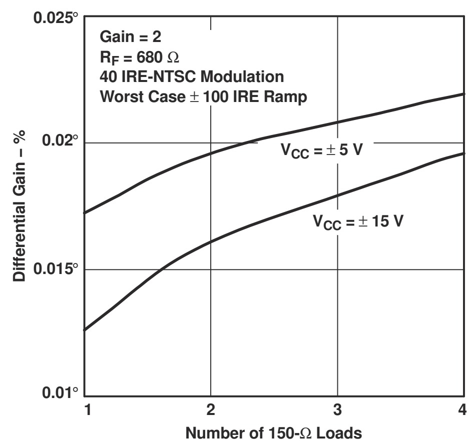


Figure 5-71. Differential Gain vs Number of 150-Ω Loads

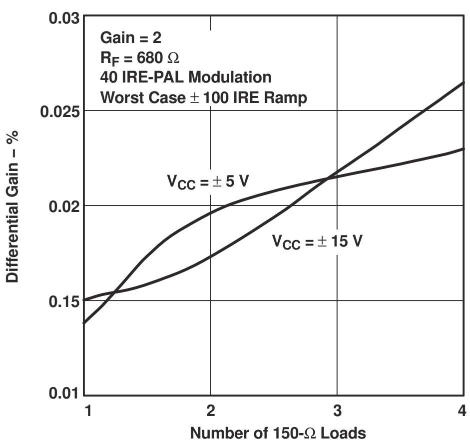


Figure 5-72. Differential Gain vs Number of 150-Ω Loads

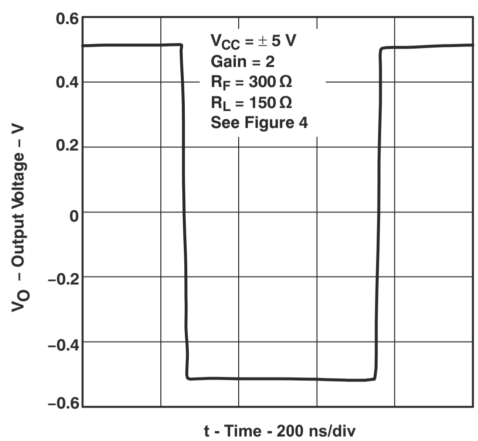


Figure 5-73. 1-V Step Response

5.11 Typical Characteristics - THS4032 (continued)

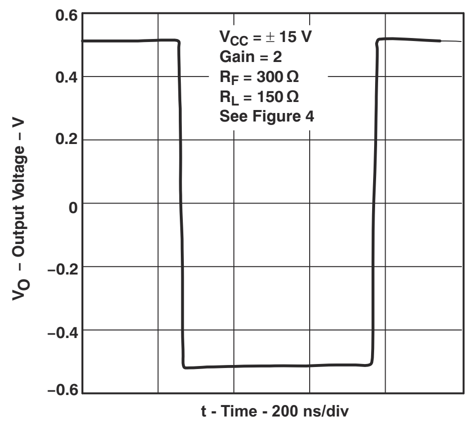


Figure 5-74. 1-V Step Response

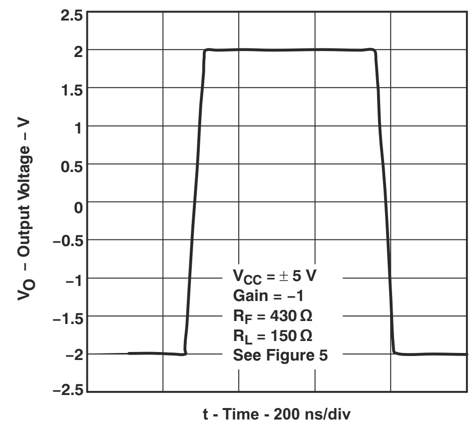


Figure 5-75. 4-V Step Response

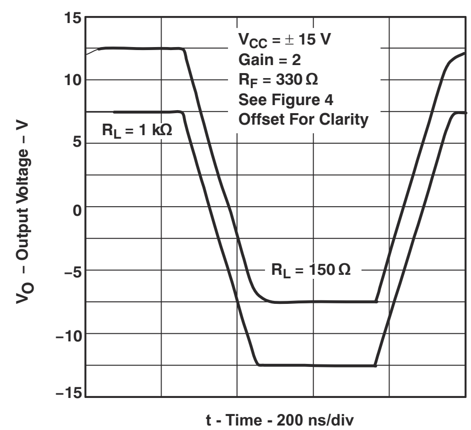


Figure 5-76. 20-V Step Response

6 Detailed Description

6.1 Overview

The THS403x are high-speed operational amplifiers configured in a voltage-feedback architecture. These amplifiers are built using a 30-V, complementary bipolar process with NPN and PNP transistors that possess an f_T of several GHz. This configuration results in exceptionally high-performance amplifiers with wide bandwidth, high slew rate, fast settling time, and low distortion.

6.2 Functional Block Diagrams

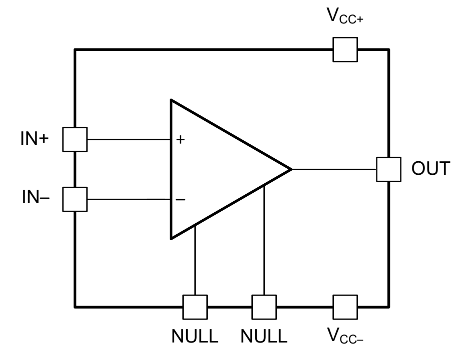


Figure 6-1. THS4031: Single Channel

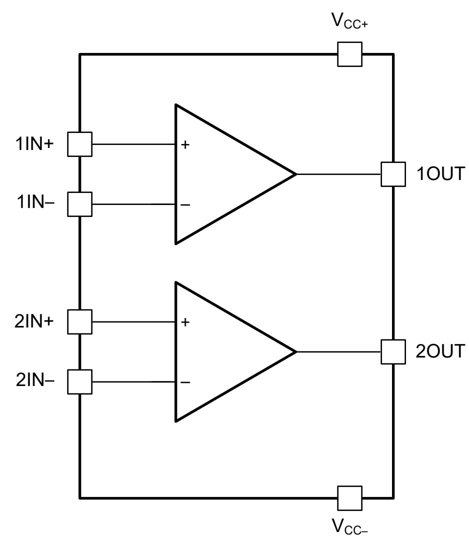


Figure 6-2. THS4032: Dual Channel

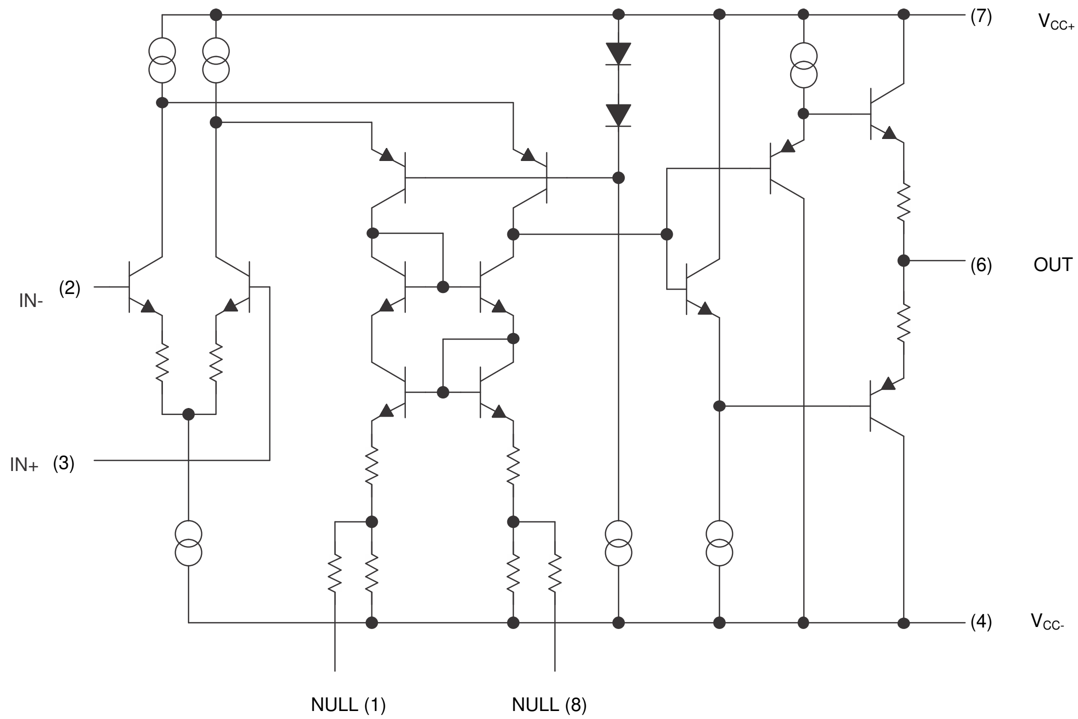


Figure 6-3. THS4031 Simplified Schematic

6.3 Feature Description

6.3.1 Offset Nulling

The THS403x have a very low input offset voltage for high-speed amplifiers. However, if additional correction is required, an offset nulling function has been provided on the THS4031. To adjust the input offset voltage, place a potentiometer between pin 1 and pin 8 of the device, and tie the wiper to the negative supply. Figure 6-4 shows this feature.

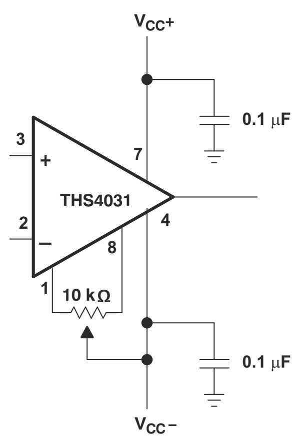


Figure 6-4. Offset Nulling Schematic

6.4 Device Functional Modes

The THS403x family has a single functional mode and can be used with both single-supply or split power-supply configurations. The power-supply voltage must be greater than 9 V (±4.5 V) and less than 33 V (±16.5 V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Driving a Capacitive Load

The THS403x devices are internally compensated to maximize bandwidth and slew-rate performance. Take additional precautions when driving capacitive loads with a high-performance amplifier to maintain stability. As a result of the internal compensation, significant capacitive loading directly on the output node decreases the device phase margin, and potentially leads to high-frequency ringing or oscillations. Therefore, for capacitive loads greater than 10 pF, place an isolation resistor in series with the output of the amplifier. Figure 7-1 shows this configuration. For most applications, a minimum resistance of 20 Ω is recommended. In 75-Ω transmission systems, setting the series resistor value to 75 Ω is a beneficial choice because this value isolates any capacitance loading and provides source impedance matching.

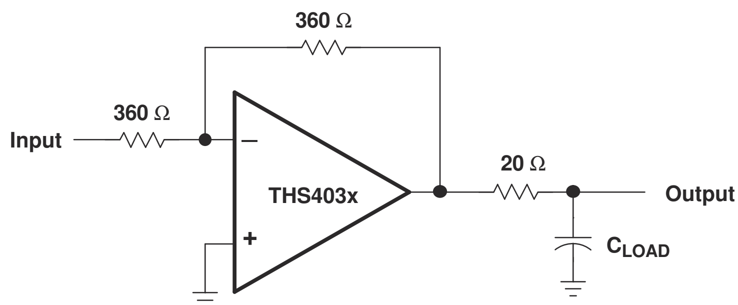


Figure 7-1. Driving a Capacitive Load

7.1.2 Low-Pass Filter Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. Figure 7-2 shows that the simplest way to accomplish this limiting is to place an RC filter at the noninverting pin of the amplifier.

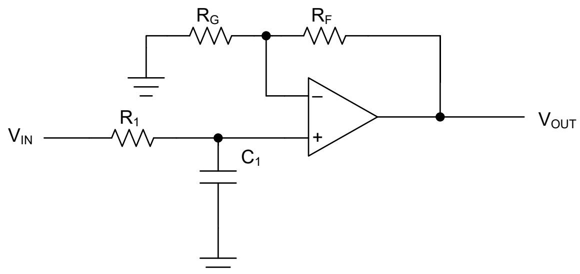


Figure 7-2. Single-Pole Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \times \left(\frac{1}{1 + sR_1C_1}\right) \tag{1}$$

If more attenuation at higher frequencies is required, a multiple-pole filter is required. Figure 7-3 shows a common implementation of a second-order filter called a Sallen-Key filter. When designing this type of filter, chose an amplifier who bandwidth is approximately an order of magnitude larger than the desired filter bandwidth. See Active Low-pass Filter Design for more detailed active-filter design information.

Assuming $R_1 = R_2 = R$ and $C_1 = C_2 = C$, use Equation 2 to set the bandwidth of the filter.

$$f_{3dB} = \frac{1}{2\pi RC} \tag{2}$$

The Q-factor of a filter controls the amount of peaking of the small-signal frequency response and the settling time of the pulse response. Set Q to 0.707 to provide a Butterworth response with a maximally flat pass band. Use Equation 3 to chose the ratio of R_F and R_G to obtain the desired Q value.

$$\frac{R_F}{R_G} = 2 - \frac{1}{Q} \tag{3}$$

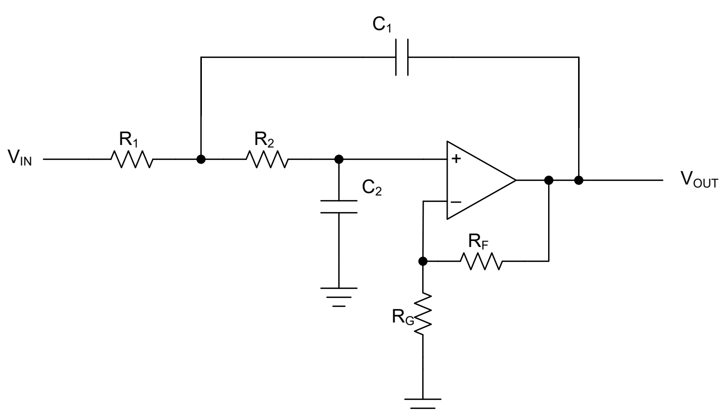


Figure 7-3. Two-Pole Low-Pass Sallen-Key Filter

7.2 Typical Application

This section demonstrates multiplexing several analog input signals to a high-performance driver amplifier which subsequently drives a single high-resolution, high-speed SAR analog-to-digital converter (ADC). This example uses the ADS8411 and the TS5A3159 or TS5A3359 as the ADC and the multiplexer, respectively. This application uses the THS403x as the operational amplifier.

As detailed in Figure 7-4, the example system consists of an ADC (ADS8411), a driving operational amplifier (THS4031), a multiplexer (TS5A3159), an ac source, a dc source, and two driving operational amplifiers.

The driving amplifiers OPA1 are OPA2 are shown as two THS4031 amplifiers. Alternatively, use a single THS4032 to save on cost and board space. The purpose of these op-amps is make the input sources present a low impedance to rest of the circuit. Additionally, to maintain signal fidelity, these operational amplifiers must have low noise and distortion. The third THS4031 labeled OPA3 in Figure 7-4 is used to maintain switching speed and drive the ADC. The passive band-pass filter before the ADC reduces unwanted noise.

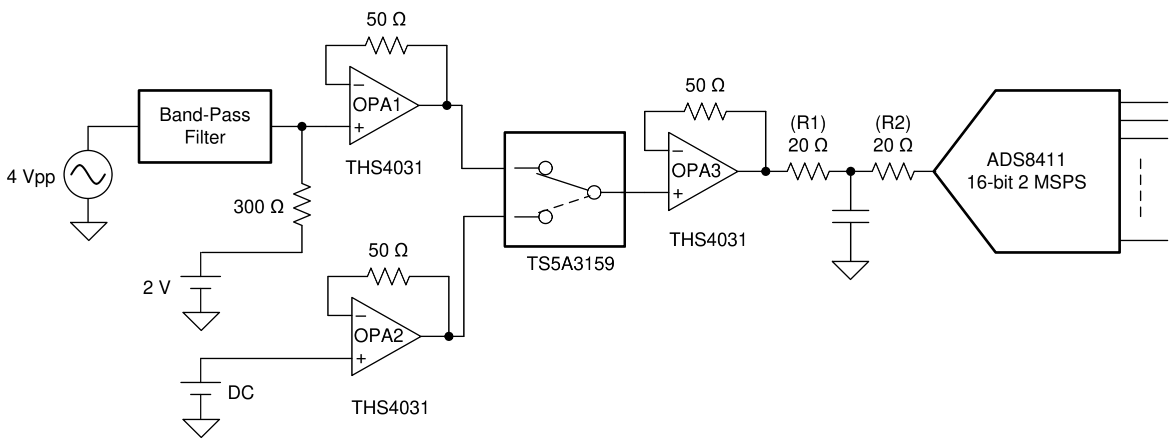


Figure 7-4. Multiplexing Setup to Drive a High-Performance ADC

7.2.1 Design Requirements

The objective to is design a multiplexed digitizer system with the dynamic performance shown in Table 7-1.

Table 7-1. Design Specifications

DEVICE SPEED (MSPS)	INPUT FREQUENCY (kHz)	SNR (dB)	THD (dB)	CROSSTALK (dB)
2	20	> 84	< –90	< –110
2	100	> 84	< –90	< –96

7.2.2 Detailed Design Procedure

The ADS8411 is a 16-bit, 2-MSPS analog-to-digital converter (ADC) with a 4-V reference. The ADS8411 has a unipolar single-ended input and includes a 16-bit capacitor-based SAR ADC, with inherent sample and hold. The output is a 16-bit parallel interface.

The TS5A3159 is a single-pole, double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The TS5A3159 offers a low ON state resistance and an excellent ON resistance matching with the break-before-make feature to prevent signal distortion during the transfer of a signal from one channel to another. Additionally, the TS5A3159 provides excellent total harmonic distortion (THD) performance and consumes low power. The TS5A3359 is a single-pole, triple-throw (SP3T) version of the same switch.

7.2.2.1 Selection of Multiplexer

Figure 7-5 shows an equivalent circuit diagram of one of the channels of a multiplexer. C_S is the input capacitance of the channel; C_D is the output capacitance of the channel. R_{ON} is the resistance of the channel when the channel is turned ON. C_L and R_L are the load capacitance and resistance, respectively. V_{IN} is the input voltage of the source. R_S is the resistance of the source. V_{OUT} is the output voltage of the multiplexer.

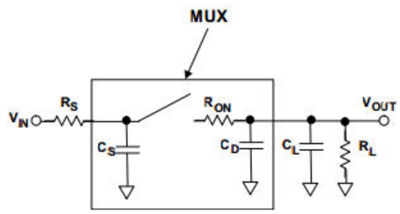


Figure 7-5. Multiplexer Equivalent Circuit

Settling time is improved when the values of R_S, R_{ON}, C_S, C_D, and C_L are small, and the value of R_L is large.

For TS5A3159:

- R_{ON} = 1 Ω
- C_S = C_D = 84 pF

Typical values for the extrinsic parameters are

- R_S = 50 Ω
- C_L = 5 pF
- R_L = 10 kΩ
- T_{RC} (time constant) = 8.65 ns

For a 16-bit system, at least 18-bit settling is desired to minimize distortion from settling artifacts. For an 18-bit settling, the circuit response time required is (18 × ln2) × T_{RC} = 108 ns, which is less than 2 MSPS sampling time of 500 ns. If the settling time is more than the conversion time of the ADC, the output of the multiplexer does not settle to the required accuracy resulting in distortion.

One more important parameter to consider when selecting a multiplexer is the on-state resistance variation with voltage. This variation also affects distortion because R_{ON} and R_L act like a resistor divider circuit. Any variation of R_{ON} with voltage affects the output voltage.

7.2.2.2 Signal Source

The input signal source must be a low-noise, low-distortion source with low source resistance. As discussed in the earlier section, the rouse resistance also must be small to avoid impacting settling time. If the source is not a low-noise and low-distortion source, a passive band-pass filter can be added to improve the signal quality as shown in Figure 7-4.

7.2.2.3 Driving Amplifier

The driving operational amplifier (OPA3 in Figure 7-4) in this application must have good slew rate, bandwidth, low noise, and distortion. The input of the operational amplifier can result in a maximum step of 4-V because of MUX switching. As a result, even if the signal bandwidth is low, the driving amplifier must settle from a 4-V step within one ADC sampling frame to avoid signal distortion. In this example, the settling requirement due to the ADC selection is 500 ns. The THS4031 is a good choice in this application due to the high slew rate and low distortion of this operational amplifier.

7.2.2.4 Driving Amplifier Bandwidth Restriction

The restriction of excess bandwidth by use of a passive RC filter before the ADC results in better SNR and THD. However, restricting the bandwidth too much results in a excessive operational amplifier settling time. If the amplifier output does not settle quick enough, some residual charge of the previous channel remains in the next sampling interval and appears as crosstalk. One approach to solve this settling issue is to reduce the throughput of the ADC. However, often the high sample rate ADC was chosen to the need to acquire higher frequency signals limiting the freedom to reduce the ADC throughput. Due to these tradeoffs, the choice of the filter capacitor becomes critical. Figure 7-6 and Figure 7-7 show SNR and crosstalk as a function of the filter capacitor.

Figure 7-8 shows input settling behavior with three different filter capacitor values. The value of the capacitor changes to filter bandwidth. As the filter bandwidth increases, the settling time improves as shown in Equation 4.

$$\text{Filter Bandwidth} \cong \frac{1}{2\pi R_1 C_1} \tag{4}$$

7.2.3 Application Curves

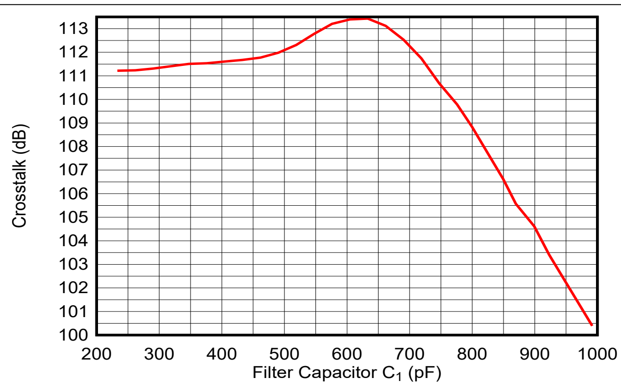


Figure 7-6. SNR vs Filter Capacitor

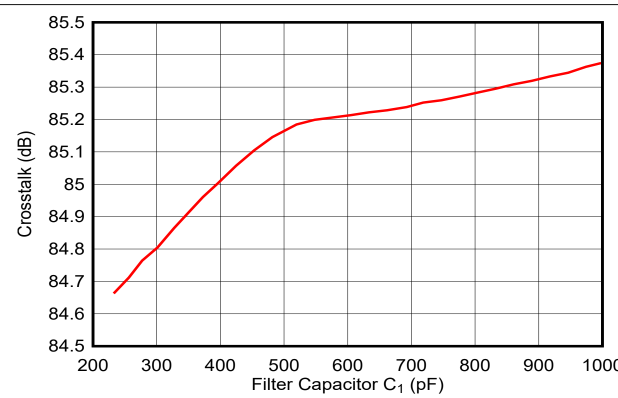


Figure 7-7. Crosstalk vs Filter Capacitor

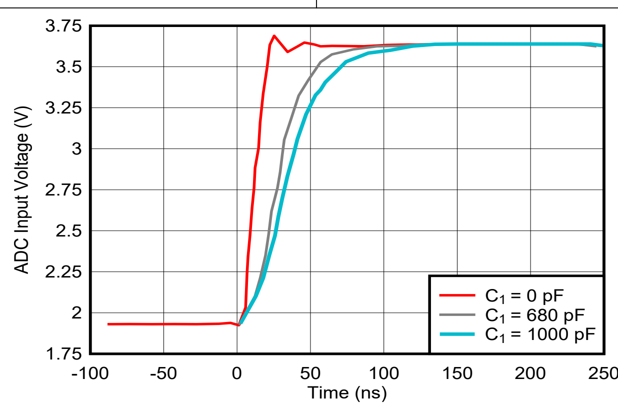


Figure 7-8. Input to ADC for Various Values of Filter Capacitors

7.3 Power Supply Recommendations

The THS403x family operates off a single supply or with dual supplies. Choose supplies that provide for the required headroom to supply rails as specified by the common-mode input range (CMIR). Operating from a single supply has numerous advantages. With the negative supply at ground, the dc errors due to the –PSRR term are minimized. Decouple supplies with low inductance capacitors to ground as close to the amplifier as possible. When operating on a board with high-speed digital signals, provide isolation between digital signal noise and the analog input pins. When using a ground plane, remove the ground plane close to input sensitive pins to reduce stray parasitics that adversely impact device performance. For split-supply operation, an optional supply decoupling capacitor across the two power supplies improves second harmonic distortion performance.

7.4 Layout

7.4.1 Layout Guidelines

To achieve the levels of high-frequency performance of the THS403x, follow proper printed-circuit board (PCB), high-frequency design techniques. The following is a general set of guidelines. In addition, a THS403x evaluation board is available to use as a guide for layout or for evaluating the device performance.

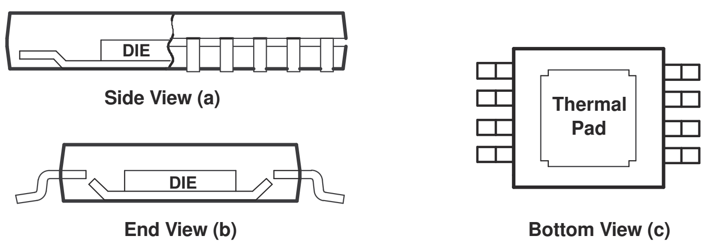
- **Ground planes**—make sure that the ground plane used on the board provides all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize stray capacitance.
- **Proper power-supply decoupling**—use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply pin. Sharing the tantalum capacitor among several amplifiers is possible depending on the application, but always use a 0.1-µF ceramic capacitor on the supply pin of every amplifier. In addition, place the 0.1-µF capacitor as close as possible to the supply pin. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. Strive for distances of less than 0.1 inch (2.54 mm) between the device power pins and the ceramic capacitors.
- **Short trace runs or compact part placements**—optimum high-frequency performance is achieved when stray series inductance is minimized. To minimize stray inductance, make the circuit layout as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inputs of the amplifier, keeping the trace lengths as short as possible. This layout helps to minimize stray capacitance at the input of the amplifier.
- **Sockets**—TI does not recommend sockets for high-speed operational amplifiers. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs and compact part placements**—Improved high-frequency performance is achieved when stray series inductance is minimized. To reduce stray series inductance, the circuit layout must be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention must be paid to the inverting input of the amplifier. The length must be kept as short as possible to minimize stray capacitance at the input of the amplifier.

7.4.1.1 General PowerPAD™ Integrated Circuit Package Design Considerations

The THS403x are available in a thermally-enhanced DGN package, which is a member of the PowerPAD™ integrated circuit package family. This package is constructed using a downset lead frame upon which the die is mounted [see Figure 7-9(a) and Figure 7-9(b)]. This arrangement results in the lead frame exposed as a thermal pad on the underside of the package [see Figure 7-9(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD integrated circuit package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are soldered), the thermal pad can be soldered to a copper area under the package. By using thermal paths within this copper area, heat is conducted away from the package into a ground plane or other heat-dissipating device.

The PowerPAD integrated circuit package represents a breakthrough in combining the small area and ease of assembly of surface mount with the more-recent, awkward mechanical methods of sinking heat.



Note: The thermal pad is electrically isolated from all pins in the package.

Figure 7-9. Views of Thermally-Enhanced DGN Package

Although there are many ways to properly dissipate heat from this device, the following steps show the recommended approach.

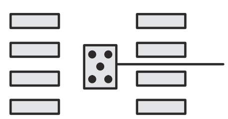


Figure 7-10. PowerPAD™ PCB Etch and Via Pattern

1. Prepare the PCB with a top-side etch pattern as shown in Figure 7-10. There must be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes must be 13 mils (0.3302 mm) in diameter. The reason to keep the holes small is to discourage solder wicking through the holes during reflow.
3. Additional vias can be placed anywhere along the thermal plane outside of the thermal pad area. This action helps dissipate the heat generated by the THS403x device. The additional vias can be of any diameter because wicking is not a concern outside of the thermal pad area.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS403x package must connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask must leave the pins of the package and the thermal pad area with the five holes exposed. The bottom-side solder mask must cover the five holes of the thermal pad area, which prevents solder from pulling away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the device pins.
8. With these preparatory steps in place, the THS403x device is placed in position and run through the solder reflow operation as any standard surface-mount component.

7.4.2 Layout Example

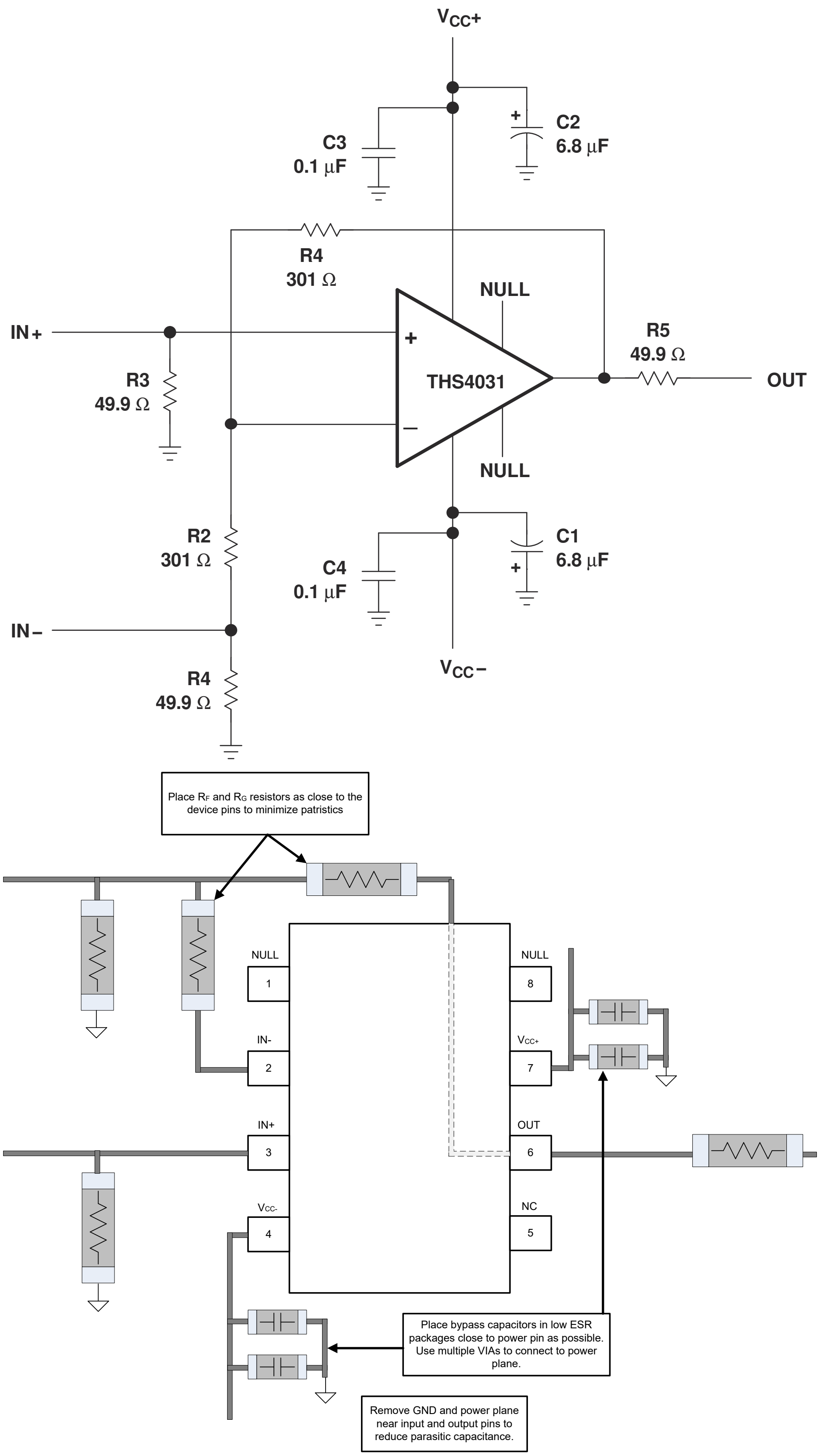


Figure 7-11. Layout Recommendations

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Noise Analysis for High-Speed Op Amps*, application report
- Texas Instruments, *PowerPAD™ Thermally-Enhanced Package*, application report
- Texas Instruments, *THS4031 High-Speed Op Amp*, EVM user's guide
- Texas Instruments, *THS4032 Dual High-Speed Op Amp*, EVM user's guide

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (February 2024) to Revision K (May 2024) **Page**

- Deleted Total harmonic distortion + noise and Intermodulation distortion specifications from *Electrical Characteristics - THS4031, R_L = 150 Ω* 6
- Deleted Total harmonic distortion + noise and Intermodulation distortion specifications from *Electrical Characteristics - THS4031, R_L = 1 kΩ* 7
- Changed gain from +2 V/V to +1 V/V in *Typical Characteristics - THS4031* 12
- Changed abscissa axis label from 10 ns/div to 100 ns/div in Figure 5-23, *20V Step Response* 12

Changes from Revision I (May 2018) to Revision J (February 2024) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document........ 1
- Changed table note 1 in *Absolute Maximum Ratings* to add additional clarification........ 4
- Changed output current max in *Absolute Maximum Ratings* from 150 mA to 240 mA........ 4

- Changed differential supply voltage in *Absolute Maximum Ratings* from ± 4 V to ± 1.5 V....4
- Added continuous input current in *Absolute Maximum Ratings* 4
- Deleted M-suffix temperature range and in *Absolute Maximum Ratings* 4
- Deleted JG and FK package references in *Absolute Maximum Ratings* 4
- Changed charged-device model (CDM) reference from JESD22-C101 to JS-002 in *ESD Ratings* 4
- Updated *Thermal Information: THS4031* for the D and DGN packages.... 5
- Deleted full-power bandwidth specification from *Electrical Characteristics - THS4031, R_L = 150 Ω* 6
- Added *Electrical Characteristics - THS4031, RL = 150* Ω section.... 6
- Changed bandwidth for 0.1-dB flatness in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 50 MHz to 9 MHz for V_{CC} = ±15 V....6
- Changed bandwidth for 0.1-dB flatness in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 45 MHz to 9 MHz for V_{CC} = ±5 V....6
- Changed settling time to 0.1% in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 60 ns to 70 ns for V_{CC} = ±15 V....6
- Changed settling time to 0.1% in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 45 ns to 55 ns for V_{CC} = ±5 V....6
- Deleted total harmonic distortion for 1 kΩ in *Electrical Characteristics - THS4031, R_L = 150 Ω* 6
- Changed input voltage noise - in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 1.6 nV/√Hz to 1.2 nV/√Hz.... 6
- Changed input current noise in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 1.2 pA/√Hz to 2.3 pA/√Hz.... 6
- Changed open loop gain condition in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 1 kΩ to 150 Ω...6
- Changed open loop gain minimum in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 98 dB to 100 dB for V_{CC} = ±15 V, T_A = 25 °C....6
- Changed open loop gain minimum specification in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 95 dB to 98 dB for VCC = ±5 V, TA = 25 °C.... 6
- Updated input offset voltage values and units specification in *Electrical Characteristics - THS4031, R_L = 150 Ω* 6
- Added input offset current specification in *Electrical Characteristics - THS4031, R_L = 150 Ω* table.... 6
- Changed common-mode input voltage range typical in *Electrical Characteristics - THS4031,R_L = 150 Ω* from ±14 V to ±14.3 V for V_{CC} = ±15 V....6
- Changed common-mode input voltage range typical in *Electrical Characteristics - THS4031, R_L = 150 Ω* from ±4 V to ±4.3 V for V_{CC} = ±5 V.... 6
- Deleted output voltage swing for R_L = 1 kΩ in *Electrical Characteristics - THS4031, R_L = 150 Ω* 6
- Changed output voltage swing condition for V_{CC} = ±15 V in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 150 Ω to 250 Ω....6
- Changed output voltage swing condition for V_{CC} = ±5 V in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 250 Ω to 150 Ω....6
- Deleted short circuit current in *Electrical Characteristics - THS4031, R_L = 150* Ω 6
- Changed output current load resistance typical in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 20 Ω to 10 Ω....6
- Changed output current typical in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 90 mA to 200 mA for V_{CC} = ±15V....6
- Changed output current typical in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 70 mA to 160 mA for V_{CC} = ±5V....6
- Changed output resistance typical in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 13 Ω to 5 Ω...... 6
- Changed supply current (each amplifier) typical in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 8.5 mA to 7.5 mA for V_{CC} = ±15 V....6
- Changed supply current (each amplifier) typical in *Electrical Characteristics - THS4031, R_L = 150 Ω* from 7.5 mA to 6.5 mA for V_{CC} = ±5 V....6
- Changed bandwidth for 0.1-dB flatness in *Electrical Characteristics - THS4031 , R_L = 1 kΩ* from 50 MHz to 9 MHz for V_{CC} = ±15 V....7

- Changed bandwidth for 0.1-dB flatness in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 45 MHz to 9 MHz for V_{CC} = ±5 V..... 7
- Changed full power bandwidth calculation from slew rate / [$\sqrt{\pi}V_{OC(Peak)}$] to slew rate / [$\pi V_{O(P-P)}$] in *Electrical Characteristics - THS4031, R_L = 1 kΩ* 7
- Changed full power bandwidth in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 2.3 to 1.6 for V_{CC} = ±15 V..... 7
- Changed full power bandwidth specification in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 7.1 to 5.1 for V_{CC} = ±5 V..... 7
- Changed 0.1% setting time in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 60 to 70 for V_{CC} = ±15 V 7
- Changed 0.1% setting time in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 45 to 55 for V_{CC} = ±15 V..... 7
- Deleted total harmonic distortion, voltage noise, current noise, differential gain error, and differential phase error for R_L = 150 Ω in *Electrical Characteristics - THS4031, R_L = 1 kΩ* 7
- Changed open loop gain minimum in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 98 dB to 100 dB for VCC = ±15 V, T_A = 25 °C..... 7
- Changed open loop gain minimum in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 95 dB to 98 dB for V_{CC} = ±5 V, T_A = 25 °C..... 7
- Changed input offset voltage typical in *Electrical Characteristics - THS4031, R_L = 1k Ω* from 0.5 mV to 0.3 mV..... 7
- Changed input bias current typical in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 3 µA to 9 µA for T_A = 25°C..... 7
- Changed input bias current max in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 6 µA to 20 µA for T_A = 25°C..... 7
- Changed input bias current max in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 8 µA to 33 µA for T_A = full range..... 7
- Deleted output voltage swing for R_L = 150 Ω and R_L = 250 Ω in *Electrical Characteristics - THS4031, R_L = 1 kΩ* table..... 7
- Deleted output current in *Electrical Characteristics - THS4031, R_L = 1 kΩ* table..... 7
- Deleted output resistance in *Electrical Characteristics - THS4031, R_L=1 kΩ*..... 7
- Changed supply current (each amplifier) typical in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 8.5 mA to 7.5 mA for V_{CC} = ±15 V..... 7
- Changed supply current (each amplifier) in *Electrical Characteristics - THS4031, R_L = 1 kΩ* from 7.5 mA to 6.5 mA for V_{CC} = ±5 V..... 7
- Deleted full-power bandwidth specification from *Electrical Characteristics - THS4032, R_L = 150Ω* 9
- Changed title of *Electrical Characteristics - R_L = 150Ω* to *Electrical Characteristics - THS4032, R_L = 150Ω* ... 9
- Updated input offset voltage units specification in *Electrical Characteristics - THS4032, R_L = 150Ω* 9
- Deleted 1kΩ open loop gain specification from in *Electrical Characteristics - THS4032, R_L = 150Ω* 9
- Changed title of *Electrical Characteristics: R_L = 1kΩ* to *Electrical Characteristics - THS4032 R_L = 1kΩ* 10
- Deleted 150Ω input voltage noise, input current noise, differential gain error, and differential phase error, specifications from *Electrical Characteristics - THS4032, R_L = 1kΩ* 10
- Deleted output voltage swing for R_L = 150Ω and R_L = 250Ω in *Electrical Characteristics - THS4032, R_L = 1kΩ table* 10
- Added *Typical Characteristics - THS4031* section..... 12
- Changed title of *Typical Characteristics* to *Typical Characteristics - THS4032* 18
- Deleted *Parameter Measurement Information* section..... 26
- Deleted *Noise Calculation and Noise Figure*, *Optimizing Frequency Response*, and *Offset Voltage* sections 27
- Changed *Application Information* section to latest standard format..... 28
- Changed name of *General Configuration* section to *Low-pass Filter Configurations* 29
- Deleted thermal calculations in *General PowerPAD™ Integrated Circuit Package Design Considerations* ... 34

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265