

Features

- Contactless Power Supply
- Contactless Read/Write Data Transmission
- Radio Frequency f_{RF} from 100 kHz to 150 kHz
- 128-bit EEPROM User Memory: 16 Bytes (8 Bits Each)
- 8-bit Configuration Memory
- High Q-antenna Tolerance Due to Built-in Options
- Applications
 - Access Control
 - Standard Unique Format (Manchester, RF/64)
 - 40-bit Data Memory
 - 14-bit Parity Memory
 - 9-bit Header Memory
- On-chip Trimmed Antenna Capacitor
 - 330 pF $\pm 3\%$
 - 250 pF $\pm 3\%$
- Mega Pads $200 \mu\text{m} \times 400 \mu\text{m}$
- Mega Pads $200 \mu\text{m} \times 400 \mu\text{m}$ with 25 μm Gold Bumps for Direct Coil Bonding
- Other Options:
 - Direct Access Mode
 - OTP Functionality

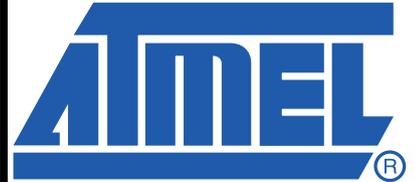
1. Description

The ATA5575 is a contactless read/write identification IC (IDIC[®]) for applications in the 100-kHz to 150-kHz frequency band. A single coil connected to the chip serves as the IC's power supply and bi-directional communication interface. The antenna and chip together form a transponder or tag.

The on-chip 128-bit user EEPROM (16 bytes with 8 bits each) can be read and written byte-wise from a base station (reader). Data is transmitted from the IDIC (uplink) using load modulation. This is achieved by damping the RF field with a resistive load between the two terminals Coil 1 and Coil 2. The IC receives and decodes serial base station commands (downlink), which are encoded as 100% amplitude modulated (OOK) pulse-interval-encoded bit streams.

The ATA5575 is an EEPROM-based circuit. It is optimized for maximum read range. Programming is also possible, but the write range is limited.

The chip has to be locked after loading the application-specific data into the device. Until the enable bits are set properly, the ATA5575M1 transmits all digits "0" in unique format. Typical applications run at 125 kHz.



**Read/Write
LF RFID IDIC
100 kHz to
150 kHz**

ATA5575M1

Summary

Preliminary

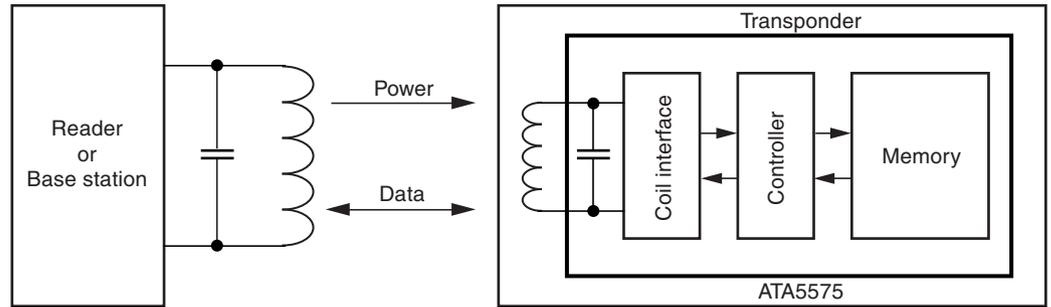
NOTE: This is a summary document. The complete document is available. For more information, please contact your local Atmel sales office.

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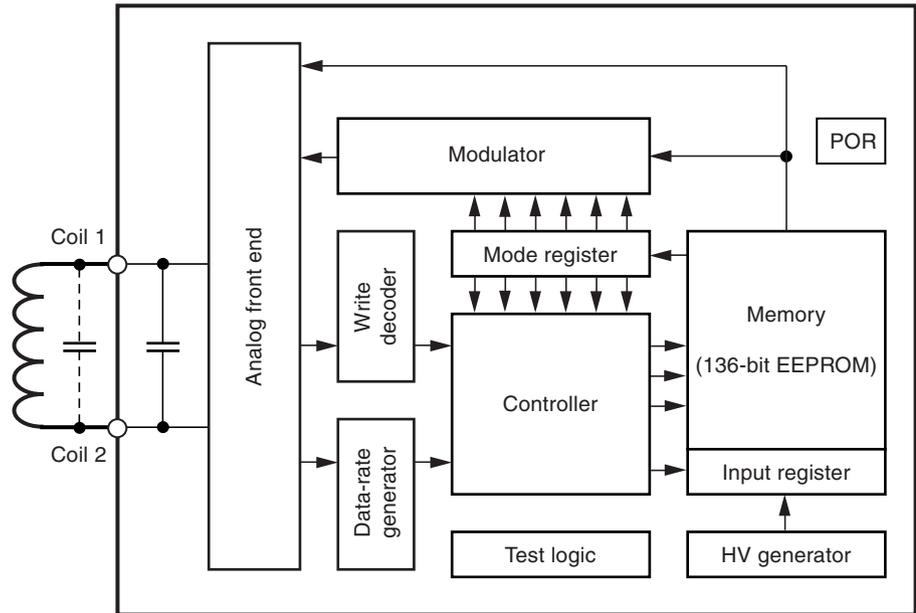
2. System Block Diagram

Figure 2-1. RFID System Using ATA5575 Tag



3. ATA5575 - Functional Blocks

Figure 3-1. Block Diagram



4. Analog Front End (AFE)

The AFE includes all circuits which are directly connected to the coil terminals, it generates the IC's power supply and handles the bi-directional data communication with the reader. The AFE consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage
- Clock extractor
- Switchable load between Coil 1 and Coil 2 for data transmission from tag to the reader
- Field-gap detector for data transmission from the base station to the tag
- ESD protection circuitry

4.1 Data Rate Generator

The data rate is fixed to RF/64.

4.2 Write Decoder

The write decoder detects the write gaps and verifies the validity of the data stream according to the Atmel® downlink protocol (pulse interval encoding).

4.3 HV Generator

This on-chip charge pump circuit generates the high voltage required for programming the EEPROM.

4.4 DC Supply

Power is externally supplied to the IDIC via the two coil connections. The IC rectifies and regulates this RF source and uses it to generate its supply voltage.

4.5 Power-On Reset (POR)

The power-on reset circuit blocks the voltage supply to the IDIC until an acceptable voltage threshold has been reached. This, in turn, triggers the default initialization delay sequence. During this configuration period of 98 field clocks, the ATA5575 is initialized with the configuration data stored in EEPROM byte 16.

4.6 Clock Extraction

The clock extraction circuit uses the external RF signal as its internal clock source.

4.7 Controller

The control logic module executes the following functions:

- Load mode register with configuration data from EEPROM byte 16 after power-on and during reading
- Controls each EEPROM memory read/write access and handles the data protection
- Handle the downlink command decoding, detecting protocol violations and error conditions

4.8 Mode Register

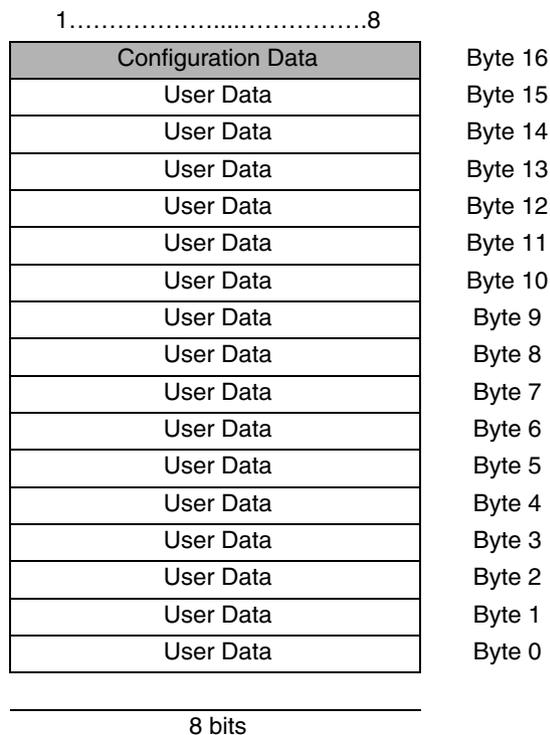
The mode register maintains a readable shadow copy of the configuration data held in byte 16 of the EEPROM. It is continually refreshed during read mode and (re-)loaded after every POR event or reset command. Depending on the version, the configuration data is pre-programmed when leaving Atmel's production.

4.9 Modulator

The modulator encodes the serialized EEPROM data for transmission to a tag reader or a base station. Modulation available: Manchester.

4.10 Memory

Figure 4-1. Memory Map



The memory is a 136-bit EEPROM, which is arranged in 17 bytes of 8 bits each. Programming is carried out byte-wise, so a complete byte will be programmed with a single command.

Byte 16 contains the mode/configuration data, which is not transmitted during regular read operations.

A special bit combination in byte 16 will lock the entire memory. Once locked, the memory (including byte 16 itself) can not be re-programmed once more via the RF field.

5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Value	Unit
Maximum DC current into Coil1/Coil2	I_{coil}	TBD	mA
Maximum AC current into Coil1/Coil2 $f = 125 \text{ kHz}$	$I_{\text{coil p}}$	TBD	mA
Power dissipation (dice) (free-air condition, time of application: 1s)	P_{tot}	TBD	mW
Electrostatic discharge maximum to ANSI/ESD-STM5.1-2001 standard (HBM)	V_{max}	TBD	V
Operating ambient temperature range	T_{amb}	-40 to +85	°C
Storage temperature range (data retention reduced)	T_{stg}	-40 to +150	°C

t

6. Electrical Characteristics

$T_{\text{amb}} = +25^{\circ}\text{C}$; $f_{\text{coil}} = 125 \text{ kHz}$; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
1	RF frequency range		f_{RF}	100	125	150	kHz	
2.1	Supply current (without current consumed by the external LC tank circuit)	$T_{\text{amb}} = 25^{\circ}\text{C}^{(1)}$	I_{DD}		1.5	3	μA	T
2.2		Read – full temperature range			2	5	μA	Q
2.3		Programming – full temperature range			25		μA	Q
3.1	Coil voltage (AC supply)	Read mode and write command ⁽²⁾	$V_{\text{coil pp}}$	6		V_{clamp}	V	Q
3.2		Program EEPROM ⁽²⁾		16		V_{clamp}	V	Q
4	Start-up time	$V_{\text{coil pp}} = 6\text{V}$	t_{startup}		1.1		ms	Q
5.1	Clamp	3 mA current into Coil1/2	V_{pp}	TBD	17	TBD	V	T
5.2		20 mA current into Coil1/2	V_{pp}	TBD	20	TBD	V	T
6.1	Modulation parameters	3 mA current into Coil1/2 and modulation ON	V_{pp}	TBD	7	TBD	V	Q
6.2		20 mA current into Coil1/2 and modulation ON	V_{pp}	TBD	9	TBD	V	T
6.3	Thermal stability		$V_{\text{mod lo}}/T_{\text{amb}}$		-1		mV/°C	Q

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

- Notes:
- I_{DD} measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
 - Current into Coil1/Coil2 is limited to 10 mA.
 - Since the EEPROM performance is influenced by assembly processes, Atmel can not confirm the parameters for -DDW (tested die on unsawn wafer) delivery.

6. Electrical Characteristics (Continued)

$T_{amb} = +25^{\circ}\text{C}$; $f_{coil} = 125\text{ kHz}$; unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit	Type*
7.1	Clock detection level	$V_{coil\ pp} = 8\text{V}$	V_{clkdet}	TBD	550	TBD	mV	T
7.2	Gap detection level	$V_{coil\ pp} = 8\text{V}$	$V_{gapdet\ med}$	TBD	550	TBD	mV	T
8	Programming time	From last command gap to re-enter read mode (64 + 648 internal clocks)	T_{prog}	5	5.7	6	ms	T
9	Endurance	Erase all / write all ⁽³⁾	n_{cycle}	100000			Cycles	Q
10.1	Data retention	$T_{op} = 55^{\circ}\text{C}^{(3)}$	$t_{retention}$	10	20	50	Years	Q
10.2		$T_{op} = 150^{\circ}\text{C}^{(3)}$	$t_{retention}$	96			hrs	T
10.3		$T_{op} = 250^{\circ}\text{C}^{(3)}$	$t_{retention}$	24			hrs	Q
11.1	Resonance capacitor	Mask option ⁽⁴⁾	C_r	TBD	330	TBD	pF	T
11.2		$V_{coil\ pp} = 1\text{V}$		TBD	250	TBD		

*) Type means: T: directly or indirectly tested during production; Q: guaranteed based on initial product qualification data

- Notes:
1. I_{DD} measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
 2. Current into Coil1/Coil2 is limited to 10 mA.
 3. Since the EEPROM performance is influenced by assembly processes, Atmel can not confirm the parameters for -DDW (tested die on unsawn wafer) delivery.



Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
rfid@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

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