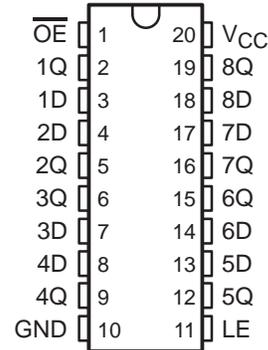


# SN54LV373, SN74LV373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

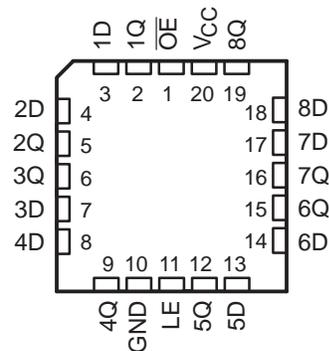
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- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8\text{ V}$  at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2\text{ V}$  at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

SN54LV373 . . . J OR W PACKAGE  
SN74LV373 . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LV373 . . . FK PACKAGE  
(TOP VIEW)



## description

These octal transparent D-type latches are designed for 2.7-V to 5.5-V  $V_{CC}$  operation.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV373 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV373 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV373 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

FUNCTION TABLE  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z



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 **TEXAS  
INSTRUMENTS**

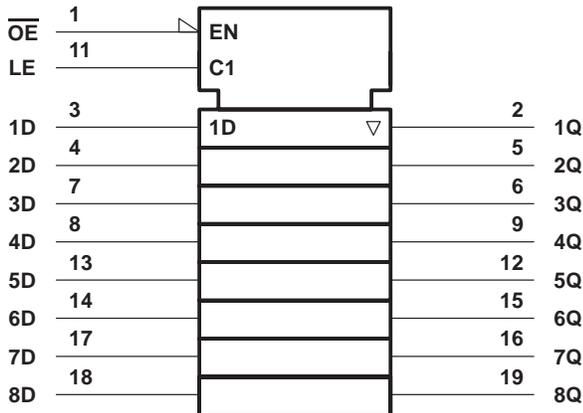
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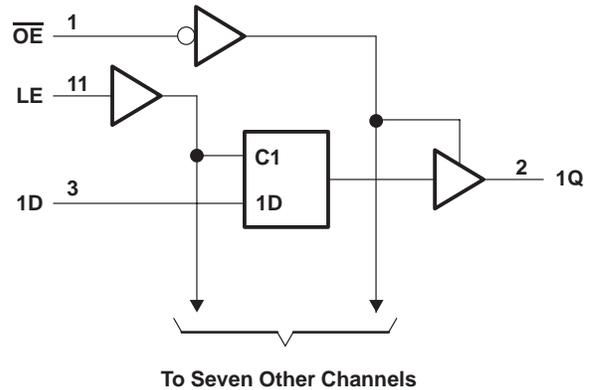
# SN54LV373, SN74LV373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## logic symbol†



## logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DB, DW, J, PW, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND	$\pm 70$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3):	
DB package	0.6 W
DW package	1.6 W
PW package	0.7 W
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. This value is limited to 7 V maximum.

3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

# SN54LV373, SN74LV373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 4)

		SN54LV373		SN74LV373		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	5.5	2.7	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		2		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		3.15		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		0.8		V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		1.65		
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		-8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		-16		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		8		mA
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$		16		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100	0	100	ns/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}^\dagger$	SN54LV373			SN74LV373			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$ $I_{OH} = -8\ \text{mA}$ $I_{OH} = -16\ \text{mA}$	MIN to MAX	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		3 V	2.4			2.4			
		4.5 V	3.6			3.6			
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$ $I_{OL} = 8\ \text{mA}$ $I_{OL} = 16\ \text{mA}$	MIN to MAX	0.2			0.2			V
		3 V	0.4			0.4			
		4.5 V	0.55			0.55			
$I_I$	$V_I = V_{CC}$ or GND	3.6 V	$\pm 1$			$\pm 1$			$\mu\text{A}$
		5.5 V	$\pm 1$			$\pm 1$			
$I_{OZ}$	$V_O = V_{CC}$ or GND	3.6 V	$\pm 5$			$\pm 5$			$\mu\text{A}$
		5.5 V	$\pm 5$			$\pm 5$			
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20			20			$\mu\text{A}$
		5.5 V	20			20			
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND	3 V to 3.6 V	500			500			$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	3.3 V	2.5			2.5			pF
		5 V	3			3			
$C_o$	$V_O = V_{CC}$ or GND	3.3 V	7			7			pF
		5 V	7.5			7.5			

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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**SN54LV373, SN74LV373**  
**OCTAL TRANSPARENT D-TYPE LATCHES**  
**WITH 3-STATE OUTPUTS**

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN54LV373						UNIT
		V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	10		10		8		ns
t <sub>su</sub>	Setup time, data before LE↓	4		6		6		ns
t <sub>h</sub>	Hold time, data after LE↓	6		6		6		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN74LV373						UNIT
		V <sub>CC</sub> = 5 V ± 0.5 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	10		10		8		ns
t <sub>su</sub>	Setup time, data before LE↓	4		6		6		ns
t <sub>h</sub>	Hold time, data after LE↓	6		6		6		ns

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV373						UNIT		
			V <sub>CC</sub> = 5 V ± 0.5 V			V <sub>CC</sub> = 3.3 V ± 0.3 V				V <sub>CC</sub> = 2.7 V	
			MIN	TYP	MAX	MIN	TYP	MAX		MIN	MAX
t <sub>pd</sub>	D	Q	8 16			11 22			28		ns
	LE		11 19			15 25			26		
t <sub>en</sub>	$\overline{OE}$	Q	15 23			15 27			28		ns
t <sub>dis</sub>	$\overline{OE}$	Q	15 23			15 27			28		ns

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV373						UNIT		
			V <sub>CC</sub> = 5 V ± 0.5 V			V <sub>CC</sub> = 3.3 V ± 0.3 V				V <sub>CC</sub> = 2.7 V	
			MIN	TYP	MAX	MIN	TYP	MAX		MIN	MAX
t <sub>pd</sub>	D	Q	8 16			11 22			28		ns
	LE		11 19			15 25			26		
t <sub>en</sub>	$\overline{OE}$	Q	15 23			15 27			28		ns
t <sub>dis</sub>	$\overline{OE}$	Q	15 23			15 27			28		ns

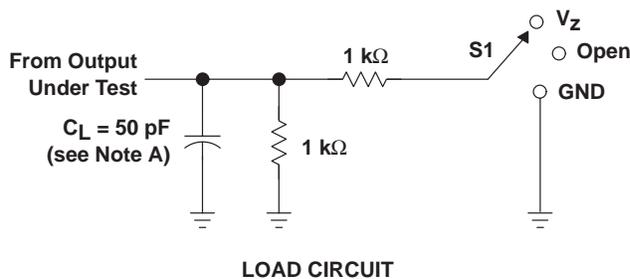
operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance per latch	Outputs enabled	C <sub>L</sub> = 50 pF, f = 10 MHz	3.3 V	47	pF
		Outputs disabled			29	
		Outputs enabled		5 V	112	
		Outputs disabled			62	

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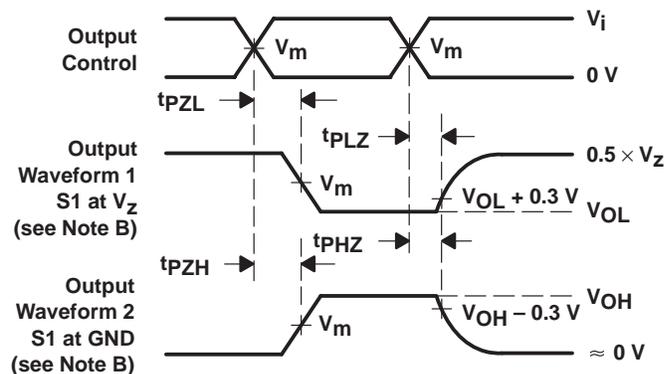
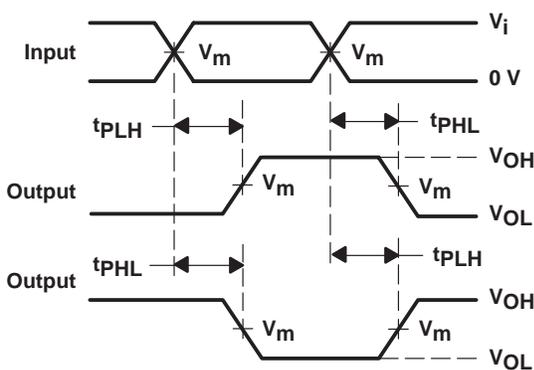
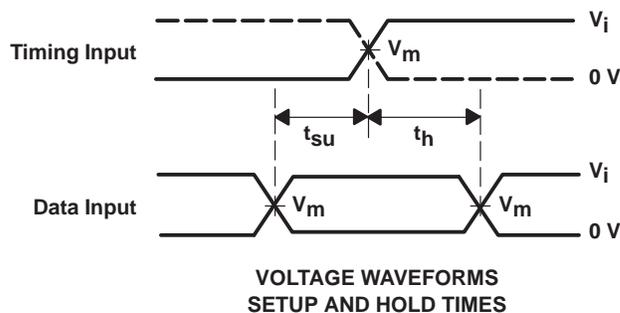
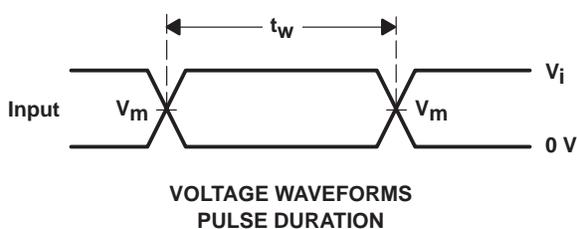


PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>Z</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

WAVEFORM CONDITION	V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> = 2.7 V to 3.6 V
V <sub>m</sub>	0.5 × V <sub>CC</sub>	1.5 V
V <sub>i</sub>	V <sub>CC</sub>	2.7 V
V <sub>Z</sub>	2 × V <sub>CC</sub>	6 V



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

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